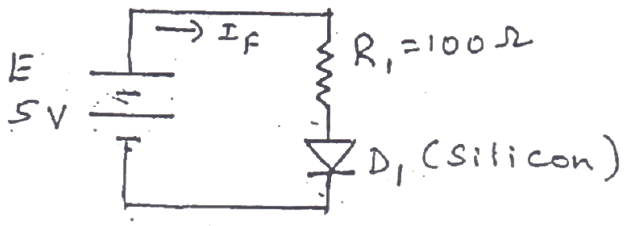
Question Bank for Basic Electronics (BBEE103/203)

Module – 1

Semiconductor Diodes

1. Explain the operation of pn junction diode under forward and reverse bias conditions with the help of V-I characteristics curve.
2. Explain V-I characteristics of a PN junction diode for both forward and reverse characteristics. ***(Feb '23 – 4M)***
3. Explain forward and reverse biasing VI characteristics of PN junction. ***(MQP '22 – 6M)***
4. Explain the forward and reverse characteristics of semiconductor diode. ***(Nov '23 – 6M, Jul '23 – 8M, MQP '22 – 8M)***
5. Explain the forward and reverse characteristics of PN junction diode (consider a silicon semiconductor). ***(Jan '24 – 6M)***
6. Explain the forward and reverse characteristics of a silicon diode. ***(MQP '22 – 8M)***
7. Draw and explain the V-I characteristics of a Ge (Germanium) diode.
8. Define following diode parameters: (i) Static resistance (ii) Dynamic resistance (iii) Knee voltage (iv) Forward voltage drop (v) Maximum forward current (vi) Reverse saturation current (vii) Reverse breakdown voltage (viii) Peak inverse voltage (PIV) (ix) Maximum power rating
9. Calculate forward and reverse resistances offered by a silicon diode with $I_F = 100$ mA and at $V_R = 50$ V. Assume V_F for silicon diode to be 0.75 V and reverse current $I_R \cong 100$ nA. ***(Jul '23 – 4M)***
10. Explain the different diode approximation with neat figures.
11. Write a note on diode approximation. Also calculate current in the circuit when a silicon diode connected in series with a resistor of 4.7kΩ is driven by a 15V dc supply. ***(Jan '24 – 6M)***
12. Find the value of the series resistance R required to drive a forward current of 1.25 mA through a Germanium diode from a 4.5 V battery. Write the circuit diagram showing all the values.
13. What is piecewise linear characteristic? With neat diagram, explain diode approximation of ideal diode and practical diode. ***(Jul '23 – 8M)***
14. Construct the piecewise linear characteristic for a silicon diode which has a 0.25 Ω dynamic resistance and a 200 mA maximum forward current.
15. What is a DC load line? With the help of neat circuit diagram and waveform, explain the procedure of constructing a DC load line for a semiconductor diode. ***(Nov '23 – 8M)***
16. With appropriate circuit diagram, explain the DC load line analysis of semiconductor diode. ***(Feb '23 – 8M)***

17. With appropriate circuit diagram, explain the DC load line analysis of semiconductor diode. Also mention the importance of bias point.
18. For the circuit shown in the figure, draw the DC load line and locate Q-point.



Diode Applications

1. What is a rectifier?
2. Explain positive half wave rectifier with input and output waveforms. ***(MQP '22 – 6M)***
3. Explain with neat diagram and waveforms, working of the half wave rectifier and also derive an expression for the efficiency and ripple factor. ***(MQP '22 – 7M)***
4. Derive the expressions for I_{dc}, V_{dc}, I_{rms}, V_{rms}, regulation, efficiency η_r, ripple factor γ and PIV of a half-wave rectifier.
5. Show that the maximum efficiency of a half wave rectifier is 40.6%.
6. Show that the ripple factor of a half wave rectifier is 1.21.
7. The input voltage to a half wave rectifier is $V = 200 \sin 50t$. If $R_L = 1\ k\Omega$ and forward resistance of the diode is $50\ \Omega$, find:
   i) The dc current through the diode
   ii) The ac or rms value of current through the circuit
   iii) The dc output voltage
   iv) The ac power input
   v) Rectifier efficiency ***(Feb '23 – 8M)***
8. A diode with $V_F = 0.7$ V is connected as a half wave rectifier. The load resistance is $500\ \Omega$ and the secondary RMS voltage is 22 V. Determine the peak output voltage and the peak load current. ***(MQP '22 – 4M)***
9. In a half wave rectifier, the input is from 30 V transformer. The load and diode forward resistances are $100\ \Omega$ and $10\ \Omega$ respectively. Calculate the I_{dc}, I_{rms}, P_{dc}, P_i, η, PIV and regulation factor.
10. A half wave rectifier from a supply 230 V, 50 Hz with a step-down transformer ratio 3:1 to a resistive load of 10 kΩ. The diode forward resistance is 75 Ω and transformer secondary is 10 Ω. Calculate the DC current, DC voltage, efficiency and ripple factor.
11. A transformer with 10:1 turns ratio is connected to a half wave rectifier with supply voltage of $220 \sin 210t$. If load and forward resistances are $500\ \Omega$ and $10\ \Omega$ respectively, calculate the average output voltage, dc output power, ac input power, rectification efficiency and peak inverse voltage.

12. With the help of neat circuit diagram and waveforms, explain the working of full wave rectifier with centre-tapped transformer. ***(Nov '23 – 8M)***

13. Explain the working of full wave rectifier with neat circuit diagram and waveforms. ***(Feb '23 – 8M, MQP '22 – 8M)***

14. With a neat circuit diagram and waveforms, explain the working of centre-tapped full wave rectifier and derive the efficiency for the same.

15. Derive the expressions for I_{dc}, V_{dc}, I_{rms}, $V_{rms,}$ regulation, efficiency η_r, ripple factor γ and PIV of a full-wave rectifier.

16. Show that the maximum efficiency of a full wave rectifier is 81.2%.

17. What is ripple factor? Show that the ripple factor of a full wave rectifier is 0.48.

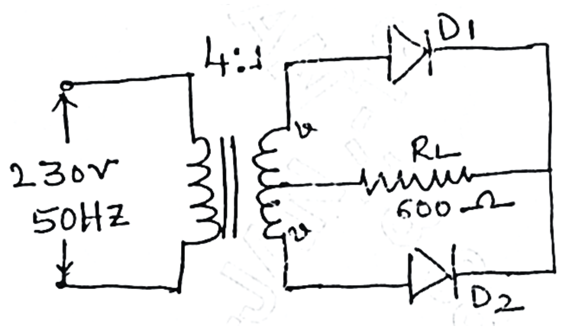
18. In a full wave rectifier, the input is from $30 - 0 - 30$ V transformer. The load and diode forward resistances are 100 Ω and 10 Ω respectively. Calculate the average load current, average load voltage and rectifier efficiency. ***(MQP '22 – 7M)***

19. A full wave rectifier has a load of 1 kΩ. The ac voltage applied to the diode is $200 - 0 - 200$ V. If diode resistance is neglected, calculate (i) average dc current (ii) average dc voltage.

20. A single phase full wave rectifier supplies power to a 1 kΩ load. The AC voltage applied to the diode is $300 - 0 - 300$ V. If diode resistance is 25Ω and that of the transformer secondary negligible, determine load current, average load voltage and rectification efficiency.

21. The input to the full wave rectifier is $v(t) = 200 \sin 50t$. If R_L is 1kΩ and forward resistance of diode is 50Ω, find:
    i) D.C current through the circuit
    ii) The A.C (rms) value of current through the circuit
    iii) The D.C output voltage
    iv) The A.C power input
    v) The D.C power output
    vi) Rectifier efficiency.

22. The input voltage applied to the primary of a 4:1 step down transformer of a full wave centre tap rectifier is 230 V, 50 Hz. If the load resistance is 600 Ω and forward resistance is 20 Ω, determine the following:
    i) dc output power
    ii) Rectification efficiency
    iii) PIV

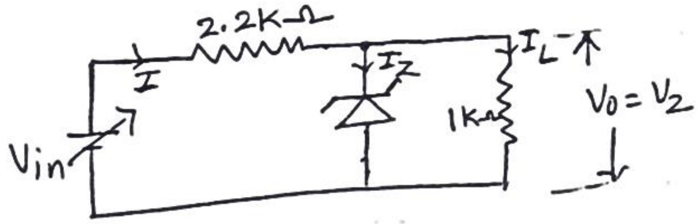


23. With neat circuit diagram and waveforms, explain the working of a bridge rectifier. ***(Jan '24 – 6M, MQP '22 – 7M)***
24. Describe the working of full wave bridge rectifier. ***(Jul '23 -8M)***
25. Derive the expressions for I_{dc}, V_{dc}, I_{rms}, $V_{rms,}$ regulation, efficiency η_r, ripple factor γ and PIV of a bridge rectifier.
26. Determine the peak output voltage and current for a bridge rectifier circuit when the secondary RMS voltage is 30 V and the diode forward drop is 0.7 V. ***(MQP '22 – 4M)***
27. What is the need for a capacitive filter? Explain.
28. Describe the working of a capacitor filter for a half wave rectifier with a neat circuit diagram and necessary waveforms. ***(Nov '23 – 8M, MQP '22 – 8M)***
29. With a neat diagram and waveforms, explain the full-wave rectifier with a capacitive filter and derive the expression for ripple factor.
30. With necessary waveform and circuit diagram, explain how a RC π-filter works. ***(Jan '24 – 6M)***
31. Explain RC π-filter. ***(MQP '22 – 8M)***
32. Illustrate RC π-filter. ***(Jul '23 – 6M)***
33. Explain the operation of RC π-filter using full wave rectifier. ***(Feb '23 – 8M)***

Zener Diodes

1. Name the junction breakdowns in diodes. Explain them briefly.
2. Distinguish between Zener and Avalanche breakdown.
3. Write down the characteristic of Zener diode. ***(MQP '22 – 4M)***
4. A Zener diode with $V_Z = 4.3$ V has $Z_Z = 20$ mA. Calculate the upper and lower limits of V_Z when I_Z changes by ± 5 mA.
5. What is Zener diode? With neat circuit diagram, explain the operation of voltage regulator with and without load. ***(Feb '23 – 4M)***
6. Explain how Zener diode can be used as a voltage regulator. ***(MQP '22 – 6M)***
7. Explain how a Zener diode can be used as voltage regulator by considering the no load and loaded conditions. ***(MQP '22 – 8M)***
8. Explain how a Zener diode works as voltage regulator considering no-load and full-load conditions. ***(Jan '24 – 8M)***
9. Explain Zener diode as voltage regulator with no load and with load. ***(Jul '23 – 6M)***
10. Explain Zener diode as voltage regulator with no load. ***(MQP '22 – 6M)***
11. A Zener diode has a breakdown voltage of 10 V. It is supplied from a voltage source varying between 20 to 40 V in series with a resistance of 820 Ω. Using an ideal Zener diode model, obtain the minimum and maximum Zener currents. ***(MQP '22 – 7M)***

12. A 9.1 V reference source is to use a series connected Zener diode and a resistor of 1 kΩ, connected to a 30 V supply. Calculate the circuit current when the supply voltage drops to 27 V. Assume $I_{ZT} = 20$ mA. Also find the power dissipated in the resistor.
(Jan '24 – 8M)
13. A 9 V reference source is to use a series connected Zener diode and a resistor connected to 30 V supply. If Zener diode with $V_Z = 9$ V, $I_{ZT} = 20$ mA is selected, then determine the value of series resistance and calculate the circuit current when the supply voltage drops to 27 V.
14. A 4.3V Zener diode is connected in series with 820 Ω resistor and DC supply voltage of 12V. Find the diode current and the power dissipation.
15. For a Zener regulator shown in the figure, calculate the range of input voltage for which output will remain constant.



$V_Z = 6.1$V, $I_{Zmin} = 2.5$mA, $I_{Zmax} = 25$mA, $r_Z = 0\Omega$.

16. Design a 6 V dc reference source to operate from a 16 V supply. The circuit is to use a low-power Zener diode with $P_D = 400$ mW and is to produce the maximum possible load current. Calculate the maximum load current that can be taken from the circuit.
17. Design Zener voltage regulator for the following specifications:
Input Voltage = 10V ± 20%, Output Voltage = 5V, $I_L = 20$mA, $I_{Zmin} = 5$mA and $I_{Zmax} = 80$mA.
18. Explain the performance of Zener diode voltage regulator in terms of source and load effects.
19. Discuss the load and line regulation using Zener diode with neat circuit diagram and appropriate expressions.
20. Define: (i) Line regulation (ii) Load regulation. ***(Nov '23 – 4M)***
21. A Zener regulator has the following data: $V_i = 16$V, $V_o = 6$V, $I_{L(max)} = 60$mA, $Z_Z = 7\Omega$, $R = 150\Omega$. Calculate line regulation and ripple rejection ratio. ***(Nov '23 – 6M)***

Module – 2
Bipolar Junction Transistors

1. With a neat diagram, explain the operation of an *npn* transistor.
2. With a neat diagram, explain the operation of a *pnp* transistor.
3. Explain various currents and voltages flowing through the BJT transistor. ***(MQP '22 – 7M)***
4. Define α and β. Determine the relationship between α and β. ***(MQP '22 – 6M)***
5. A transistor has $\beta = 150$ and I_E is 12 mA. Calculate the approximate collector current (I_C) and base current (I_B). ***(Feb '23 – 4M)***

6. Calculate I_C and I_E for a transistor that has $\alpha_{dc} = 0.98$ and $I_B = 100$ μA. Also determine the value of β_{dc} (or h_{FE}) for the transistor. ***(Jul '23 – 6M)***
7. Calculate α_{dc} and β_{dc} for the transistor if I_C is measured as 1 mA and I_B is 25 μA.
8. Describe with neat circuit diagram of BJT amplification for both voltage and current. ***(Feb '23 – 8M)***
9. Explain how transistor can be used as current amplifier. ***(Jul '23 – 6M)***
10. Explain BJT current amplification for increasing and decreasing I_B levels. ***(MQP '22 – 8M)***
11. Describe how a transistor can be used as a voltage amplifier. ***(Nov '23 – 4M, MQP '22 – 4M)***
12. Considering a BJT common emitter circuit, explain how voltage amplification is obtained. ***(Jan '24 – 6M)***
13. With a neat circuit diagram and characteristics graph, explain common base configuration of pnp transistor. ***(Jan '24 – 8M)***
14. With neat diagram, explain the input and output characteristics of transistor in common base configuration. ***(Feb '23 – 8M)***
15. Explain common base input characteristic of BJT. ***(MQP '22 – 8M, 6M)***
16. Explain the common base output characteristics. ***(Nov '23 – 8M, Jul '23 – 6M)***
17. Explain input and output characteristics of the common emitter configuration. ***(MQP '22 – 6M)***
18. Explain common emitter input characteristics. ***(Jul '23 – 6M, MQP '22 – 4M)***
19. Draw and explain output characteristics of CE configuration. ***(Nov '23 – 6M, MQP '22 – 8M)***
20. Explain common collector configuration of pnp transistor with neat circuit diagram and characteristics. ***(Jan '24 – 8M)***
21. Briefly explain common collector input characteristics. ***(Feb '23 – 4M)***
22. Explain the transistor biasing circuit with relevant expressions. ***(MQP '22 – 7M)***
23. Describe the procedure for drawing DC load line on transistor CE output characteristics. ***(Jul '23 – 8M)***
24. With respect to BJT, describe the concept of obtaining the DC load line. ***(MQP '22 – 4M)***
25. Explain how Q-point is obtained on a DC load line, considering a transistor base bias circuit. ***(Jan '24 – 6M)***
26. Draw the DC load line for transistor and identify Q point. ***(MQP '22 – 8M)***
27. For the base bias circuit, $R_C = 12k\Omega$, $R_B = 470k\Omega$, $V_{CC} = 20V$ and $V_{BE} = 0.7V$. Draw the DC load line and indicate the values. ***(Nov '23 – 6M)***

Field Effect Transistors

1. Explain the construction and operation of N-channel JFET. ***(Nov '23 – 8M, Feb '23 – 8M)***
2. Make use of N-channel JFET to describe its operation and characteristics. ***(MQP '22 – 7M)***
3. Explain the working of an N-channel JFET. ***(Jul '23 – 8M, MQP '22 – 8M, 6M)***
4. Explain the construction and operation of P-channel JFET.
5. Explain drain and transfer characteristics of N-channel JFET. ***(Jan '24 – 6M)***
6. Explain the transfer and drain characteristics of a JFET.
7. Explain the operation of enhancement MOSFET. ***(MQP '22 – 8M)***
8. With neat semiconductor model, explain how an enhancement type MOSFET works. ***(Jan '24 – 6M)***
9. Explain the construction and working of N-enhancement MOSFET. ***(Nov '23 – 8M)***
10. Make use of N-channel enhancement type MOSFET and describe the construction and working. ***(Feb '23 – 7M)***
11. Explain the enhancement type MOSFET along with the drain characteristics. ***(MQP '22 – 8M)***
12. Explain the transfer and drain characteristics of enhancement type MOSFET.
13. Explain depletion type MOSFET along with the transfer and drain characteristics. ***(Feb '23 – 8M)***

Module – 3
Operational Amplifiers

1. What is an operational amplifier? Mention its applications.
2. Explain block diagram representation of typical op-amp. ***(Nov '23 – 8M, Feb '23 – 8M, MQP '22 – 6M)***
3. Describe block diagram representation of an op-amp. Also describe its operational behavior with an equivalent circuit. ***(MQP '22 – 8M)***
4. With block diagram, explain basic structure of an op-amp. Also write its equivalent circuit diagram. ***(Jul '23 – 6M)***
5. Define the following with respect to op-amp:
   (i) Input offset voltage (ii) Input bias current (iii) CMRR (iv) Slew rate ***(Jan '24 – 8M)***
6. Explain the following terms:
   (i) Input offset current (ii) Input bias current (iii) CMRR (iv) Slew rate
   (v) Input offset voltage (vi) Voltage gain ***(Nov '23 – 6M)***
7. Define:
   (i) Input offset current (ii) Input bias current (iii) Slew rate (iv) CMRR ***(Jul '23 – 6M)***
8. Explain the following op-amp parameters:

(i) CMRR (ii) Slew rate (iii) Input offset voltage (iv) Input bias current ***(Feb '23 – 8M)***

9. With respect to an op-amp, explain the following:
   (i) Input offset voltage (ii) Slew rate ***(MQP '22 – 8M)***
10. Define Op-Amp parameters: Gain, CMRR, Slew Rate, Input resistance. ***(MQP '22 – 8M)***
11. Explain the following terms related to op-amp: (i) Open loop voltage gain (ii) Common mode gain (iii) CMRR (iv) Maximum Output Voltage Swing (v) Input Offset Voltage (vi) Input Offset Current (vii) Input bias current (viii) Input resistance (ix) Output resistance (x) Slew rate (xi) PSRR/Supply voltage rejection ratio (xii) Virtual ground.
12. A certain op-amp has an open loop voltage gain of 1,00,000 and a common mode gain of 0.2. Determine the CMRR and express it in decibels.
13. An op-amp has a slew rate of 0.8 V/μsec. What is the maximum amplitude of undistorted sine wave that the op-amp can produce at a frequency of 40 kHz? What is the maximum frequency of the sine wave that op-amp can reproduce if the amplitude is 3 V?
14. Mention all the ideal op-amp characteristics. ***(Jan '24 – 6M)***
15. List the characteristics of an ideal op-amp. ***(Nov '23 – 4M)***
16. Briefly discuss the ideal characteristics of the op-amp. ***(MQP '22 – 7M)***
17. Define op-amp. Mention any 5 ideal characteristics of an op-amp. ***(Jul '23 – 6M)***

Op-Amp Applications

1. Explain op-amp as an inverting and non-inverting amplifier. ***(Feb '23 – 8M)***
2. Explain inverting and non-inverting amplifier. ***(Jul '23 – 8M)***
3. Explain inverting amplifier. ***(MQP '22 – 4M)***
4. An inverting amplifier using op-amp has a feedback resistor of 10 kΩ and one input resistor of 1 kΩ. Calculate the gain of the op-amp and the output voltage if it is supplied with an input of 0.5 V. ***(MQP '22 – 4M)***
5. An inverting amplifier has $R_1 = 20\ k\Omega$, $R_f = 100\ k\Omega$. Find the output voltage, input resistance and input current for an input voltage of 1V.
6. Design a non-inverting amplifier circuit using op-amp, if the gain of the amplifier is 10 and input voltage is 1V. ***(Jan '24 – 6M)***
7. A non-inverting amplifier has closed loop gain of 25. If input voltage $V_i = 10$ mV, $R_f = 10\ k\Omega$, determine the value of R_1 and output voltage V_o.
8. Explain the open loop differential amplifier circuit using op-amp. Mention the advantage of negative feedback in amplifier circuit. ***(Jan '24 – 6M)***
9. Explain basic differential amplifier using op-amp. ***(Nov '23 – 8M)***
10. Explain working of a differential amplifier. ***(MQP '22 – 8M)***

11. Briefly explain op-amp as a voltage follower. ***(Feb '23 – 4M)***

12. Derive output voltage equation for 3-input inverting summer using op-amp. ***(Jan '24 – 6M)***

13. Derive an expression for the 3-input summing circuit. ***(MQP '22 – 6M)***

14. Describe a summing amplifier using an op-amp in an inverting configuration with three inputs. ***(MQP '22 – 8M)***

15. Calculate the output voltage of a three-input inverting summing amplifier, given $R_1 = 200\ k\Omega$, $R_2 = 250\ k\Omega$, $R_3 = 500\ k\Omega$, $R_f = 1\ M\Omega$, $V_1 = -2V$, $V_2 = -1V$ and $V_3 = +3V$.

16. Draw a summer circuit with $V_1 = +1\ V$, $V_2 = +3\ V$, $V_3 = +2\ V$, $R_1 = R_2 = R_3 = 2\ k\Omega$. Determine the output voltage when $R_F = 3\ k\Omega$. ***(Jul '23 – 6M)***

17. Construct an adder circuit using op-amp to obtain an output voltage of $V_o = -[2V_1 + 3V_2 + 5V_3]$. ***(Nov '23 – 6M)***

18. Design an adder circuit using an op-amp to give the output $V_o = -(3V_1 + 4V_2 + 5V_3)$. Assume $R_f = 120\ k\Omega$. ***(Feb '23 – 4M)***

19. Design the circuit diagram for the output voltage $V_o = -5(0.1V_1 + 0.2V_2 + 10V_3)$. Also draw the neat circuit diagram. ***(MQP '22 – 7M)***

20. Develop a summer circuit using op-amp to get the following output voltage $V_o = -(2V_1 + 2V_2)$. ***(MQP '22 – 4M)***

21. Design an adder circuit using op-amp to obtain an output voltage, $V_o = -[2V_1 + 3V_2 + 5V_3]$. Assume $R_f = 10\ k\Omega$.With a neat circuit diagram, explain the subtractor using an op-amp.

22. Derive an expression for integrator and differentiator. ***(MQP '22 – 6M)***

23. Describe an integrating amplifier using an op-amp in an inverting configuration. ***(Nov '23 – 8M, MQP '22 – 8M)***

24. Explain op-amp as an integrator circuit with a neat input and output waveforms using square wave as input. ***(Feb '23 – 8M, MQP '22 – 6M)***

25. Explain the working of op-amp connected as integrator. Also draw the output waveforms. ***(Jan '24 – 8M)***

26. Explain the working of op-amp as differentiator. ***(Jul '23 – 8M)***

Module – 4
Boolean Algebra and Logic Circuits

1. Convert the following numbers: ***(Jan '24 – 6M)***
   i. $(141.6875)_{10} = (?)_2$
   ii. $(125.076)_8 = (?)_{16}$
   iii. $(41F.BD)_{16} = (?)_{10}$

2. Convert the following: ***(Jan '24 – 8M)***
   i. $(FACE)_{16} = (?)_{10}$

ii. $(65.45)_{10} = (?)_2$
iii. $(1111011011011.11011)_2 = (?)_8$
iv. $(2604.10546875)_{10} = (?)_{16}$

3. Convert: ***(Jan '24 – 6M)***
i. $(456.78)_8 = (?)_2$
ii. $(642.053)_8 = (?)_{16}$

4. Convert the following: ***(Nov '23 – 6M)***
i. $(10AB)_{16} = (?)_{10}$
ii. $(240)_{10} = (?)_2$
iii. $(1234.56)_8 = (?)_{10}$

5. Convert the following binary numbers to decimal: ***(Nov '23 – 12M)***
(i) 101110 (ii) 1110101.11 (iii) 110110100

6. Convert the following: ***(Jul '23 – 8M)***
i. $(1AD.E0)_{16} = (?)_{10}$
ii. $(37.625)_{10} = (?)_2$
iii. $(110100111001.110)_2 = (?)_8$
iv. $(345.AB)_{16} = (?)_2$

7. Convert the following: ***(Jul '23 – 6M)***
i. $(2AB.8)_{16} = (?)_{10}$
ii. $(416.12)_{10} = (?)_8$
iii. $(25.375)_{10} = (?)_2$
iv. $(16.2)_8 = (?)_{16}$

8. Convert the following numbers to its equivalent numbers and show the steps: ***(Feb '23 – 6M)***
i) $(10110001101011.111100000)_2 = (?)_8$
ii) $(10110001101011.11110010)_2 = (?)_{16}$
iii) $(1010.011)_2 = (?)_{10}$

9. Convert Decimal to Binary: (i) 41 (ii)153 (iii)) 0.6875 (iv) 0.513 ***(MQP '22 – 8M)***

10. Convert Binary to Decimal: (i) 110111 (ii) 10101010 (iii) 0110 (iv) 100.1010 ***(MQP '22 – 8M)***

11. Convert the following: ***(MQP '22 – 6M)***
i. $(110.1101)_2 = (?)_{10}$
ii. $(847.951)_{10} = (?)_8$
iii. $(CAD.BF)_{16} = (?)_{10}$

12. Convert the following:
i. $(225)_{10} = (?)_2 = (?)_8 = (?)_{16}$
ii. $(11010111)_2 = (?)_{10} = (?)_8 = (?)_{16}$
iii. $(623)_8 = (?)_{10} = (?)_2 = (?)_{16}$
iv. $(2AC5)_{16} = (?)_{10} = (?)_8 = (?)_2$

13. Find the base x if $(211)_x = (152)_8$. ***(Jan '24 – 4M)***

14. Convert: ***(Nov '23 – 8M)***
    i) $(306.\text{D})_{16} = (?)_2$
    ii) $(41)_{10} = (?)_2$
    iii) Compute one's (1's) complement of $(11101)_2$
    iv) Compute 9's complement of $(0.3267)_{10}$

15. Convert the following: ***(MQP '22 – 8M)***
    a) $3\text{A}6.\text{C}58\text{D}_{(16)} = ?_{(8)}$
    b) $0.6875_{(10)} = ?_{(2)}$
    c) Compute the 9's complement of $25.639_{(10)}$
    d) Compute the 1's complement of $11101.0110_{(2)}$

16. If $\text{X} = (11011.101)_2$ and $\text{Y} = (10101.010)_2$, find $\text{X} - \text{Y}$ and $\text{Y} - \text{X}$ using 1's and 2's complements. ***(Jan '24 – 8M)***

17. Solve the following: ***(Jan '24 – 6M)***
    i) Subtract using 10's complement: $3250 - 72532$
    ii) Subtract using 2's complement: $1010100 - 1000100$

18. i) Subtract using 10's complement method: ***(Nov '23 – 6M)***
    $M = 72532, N = 03250$
    ii) Subtract using 2's complement method:
    $M = 1010100, N = 1000100$

19. Perform the following operations: ***(Jul '23 – 8M)***
    i) $1101 - 0101$ using 2's complement method
    ii) $0110 - 0010$ using 2's complement method
    iii) $924 - 126$ using 9's complement method
    iv) $265 - 424$ using 10's complement method

20. Perform the following: ***(Jan '24 – 6M)***
    i) $(1010100)_2 - (1000100)_2$ using 2's complement method.
    ii) $(4456)_{10} - (34234)_{10}$ using 10's complement method.

21. Perform the following: ***(Jul '23 – 8M)***
    i) $(1010100)_2 - (1000100)_2$ using 1's complement and 2's complement method.
    ii) $(4456)_{10} - (34234)_{10}$ using 9's complement and 10's complement method.

22. Subtract the following using 10's complement: ***(Feb '23 – 6M)***
    i) $(72532 - 3250)_{10}$
    ii) $(3250 - 72532)_{10}$

23. Perform subtraction on the given numbers using 9's complement method:
    (a) 4,637 - 2,579 (b) 125 - 1,800

24. Perform subtraction on the given numbers using 10's complement method:
    (a) 2,043 - 4,361 (b) 1,631 – 745

25. Perform subtraction on the given binary numbers using 1's complement method:
    (a) 10011 - 10010 (b) 100010 - 100110

26. Perform subtraction on the given binary numbers using 2's complement method:
 (a) 1001 - 110101 (b) 101000 - 10101
27. Subtract using (r − 1)'s complement method **(MQP '22 – 6M)**
 a) $4456_{(10)} - 34234_{(10)}$
 Subtract using r's complement method
 a) $1010100_{(2)} - 1000100_{(2)}$
28. Write down axiomatic definition of Boolean algebra. **(MQP '22 – 6M)**
29. Mention the different theorems and postulates of Boolean algebra and prove each of them with truth table. **(MQP '22 – 7M)**
30. Mention any 3 theorems of Boolean algebra and prove each of them. **(Nov '23 – 6M)**
31. Mention the postulates and theorems of Boolean algebra. **(Jul '23 – 8M)**
32. State and prove De Morgan's theorem with its truth table.
 (Jan '24 – 6M, Nov '23 – 7M, Jul '23 – 6M, MQP '22 – 5M)
33. State and prove De Morgan's theorem for 3 variables. **(Jan '24 – 6M)**
34. Using basic Boolean theorems, prove **(Feb '23 – 6M)**
 i) $(x + y)(x + z) = x + yz$
 ii) $xy + xz + y\bar{z} = xz + y\bar{z}$
35. Simplify the Boolean function to minimum number of literals: **(MQP '22 – 6M)**
 $(xy + x'y + yz)$
 $(x'y + x(y + z) + y'z')$
36. Simplify the following Boolean functions to minimum number of literals:
 i) $x + x'y$
 ii) $x(x' + y)$
 iii) $x'y'z + x'yz + xy'$
 iv) $xy + x'z + yz$
 v) $(x + y)(x' + z)(y + z)$
37. Simplify the following: **(Nov '23 – 6M)**
 i) $x(x' + y)$
 ii) $xy + x'z + yz$
38. Simplify the following Boolean expressions: **(Nov '23 – 8M)**
 i) $f(w, x, y, z) = x + xyz + \bar{x}yz + wx + \bar{w}x + \bar{x}y$
 ii) $f = \overline{(A + \bar{B} + C) + (\bar{A} + \bar{B} + C) + (\bar{A} + B)}$
39. Simplify the following expressions using Boolean Algebra: **(Jul '23 – 7M)**
 i. $\bar{A}BC + AB\bar{C} + AB$
 ii. $A + BC + B$
40. Simplify the following: **(MQP '22 – 6M)**
 i. $Y = AB + \bar{A}C + BC$
 ii. $Y = (A + \bar{B} + \bar{B})(A + \bar{B} + C)$
 iii. $Y = C(B + C)(A + B + C)$

41. Find the complement of the functions: ***(Jan '24 – 6M)***
    i) $F_1 = \overline{X}\,Y\,\overline{Z} + \overline{X}\,\overline{Y}\,Z$
    ii) $F_2 = X(\overline{Y}\,\overline{Z} + Y\,Z)$
    Apply De Morgan's theorem as many times as necessary.
42. Find the complement of the functions ***(Jul '23 – 8M)***
    i) $F_1 = x'yz' + x'y'z$
    ii) $F_2 = x(y'z' + yz)$
    using De Morgan's theorem.
43. Minimize the following function ***(MQP '22 – 7M)***
    a) $F(x, y, z) = xy + x'z + yz$
    Find the complement of the function F1 and F2
    $F1(x, y, z) = x'yz' + x'y'z$
    $F2(x, y, z) = x(y'z' + yz')$
44. Express the Boolean function
    i) $F = A + \overline{B}C$ in a sum of minterms form
    ii) $F = xy + \bar{x}z$ in a product of maxterms form ***(Feb '23 – 8M)***
45. Express the Boolean function $F = A + \overline{B}C$ in a sum of minterms form.
    (Nov '23 – 6M, Jul '23 – 6M)
46. Express the Boolean function $F = A + B'C$ in a sum of minterms. ***(Jul '23 – 6M)***
47. Express the Boolean function $F = A + BC$ in a sum of minterms. ***(MQP '22 – 6M)***
48. Express the Boolean function $F = xy + x'z$ in a product of maxterms.
49. Express the Boolean function $F = xy + \bar{x}z$ in a product of maxterms form.
    (Jan '24 – 6M, Jul '23 – 6M, MQP '22 – 6M)
50. Explain SOP and POS with examples. ***(Nov '23 – 6M, MQP '22 – 6M)***
51. Represent $F = xy + \bar{x}z$ in canonical POS form. ***(Jan '24 – 6M)***
52. What are logic gates? Write the graphic symbol, algebraic function and truth table of all 8 logic gates. ***(Nov '23 – 20M)***
53. Explain all the logic gates with the symbols and truth tables.
54. Describe how NAND and NOR gates can be used as universal gates. ***(MQP '22 – 8M)***
55. Implement the Boolean functions using logic gates: ***(Jan '24 – 6M)***
    (i) $F_1 = x + y'z$ (ii) $F_2 = x'y'z + x'yz + xy'$
56. Implement the following Boolean functions by using logic gates: ***(Jul '23 – 6M)***
    (i) $F_1 = xy' + x'z$ (ii) $F_2 = x'y'z + x'yz + xy'$

Combinational Logic

1. Write the step-by-step procedure to design a combinational circuit.
   (Jan '24 – 6M, Feb '23 – 6M)
2. Implement half adder using basic gates. ***(Nov '23 – 6M, MQP '22 – 6M)***

3. Explain the working of half adder. ***(Jul '23 – 6M)***

4. Design a half adder with necessary logic diagram and expressions. ***(Jul '23 – 5M)***

5. Define combinational circuit. Design a half adder and implement using NAND gates. ***(Jan '24 – 8M)***

6. Explain the design procedure for combinational logic circuits and implement full adder using basic gates. ***(Jan '24 – 10M)***

7. Design a full adder and implement using basic gates. ***(Jan '24 – 8M)***

8. With the help of truth table, explain the operation of full adder with sum and carry expressions, along with circuit diagram. ***(Nov '23 – 7M)***

9. Explain full adder circuit with truth table. Realize the circuit for sum and carry using basic gates. ***(Nov '23 – 8M)***

10. With the help of truth table explain the operation of full adder with its circuit diagram and reduce the expression for sum and carry. ***(MQP '22 – 7M)***

11. Describe the working of the full adder using basic gates. ***(MQP '22 – 8M)***

12. Explain the working of full adder. ***(Jul '23 – 6M)***

13. With the help of truth table, explain full adder using logic gates. ***(Aug '22 – 6M, Feb '22 – 8M, MQP '21 – 5M)***

14. Implement full adder circuit with its truth table and draw the logic diagram of sum and carry. ***(Jan '24 – 8M)***

15. Implement full adder circuit with its truth table and write the expressions for sum and carry. ***(Jul '23 – 6M)***

16. Implement full adder using two half adders and one OR gate. Write the equations for Sum and C_{out}. ***(Feb '23 – 8M)***

17. Design a full adder circuit using two half adders. ***(Jul '23 – 8M)***

18. Design a full adder using two half adders and an OR-gate. ***(MQP '21 – 8M)***

Module – 5
Introduction to Transducers

1. Explain the working of the potentiometric resistive transducer with neat diagram. ***(Nov '23 – 8M, MQP '22 – 8M)***

2. With neat diagram, explain potentiometer type resistive transducer. Also mention the applications of it. ***(Jan '24 – 8M)***

3. Explain potentiometric type transducer. ***(MQP '22 – 6M)***

4. What are the two types of strain gauges? Explain with neat diagrams.

5. A strain gauge with gauge factor of 2 is subject to a 0.28 mm strain. The wire dimensions are 50 cm length and 30 μm diameter, and unstrained wire resistance is 55 Ω. Calculate the

change in wire resistance and diameter if the entire length of the wire is strained positively. ***(MQP '22 – 7M)***

6. A strain gauge with a 40 cm wire length and a 25 μm wire diameter has a resistance of 250Ω and a gauge factor of 2.5. Calculate the change in wire length and diameter when the resistance change is measured as 0.5 Ω. Assume that the complete length of wire is strained positively. ***(Jan '24 – 6M)***
7. With a neat diagram, explain the working of a variable reluctance transducer.
8. The coil in a variable reluctance transducer has a 1 mH inductance when the total air gap length is 1 mm. Calculate the inductance change when the air gap is reduced by 0.2 mm. ***(Feb '23 – 4M)***
9. Describe the working of a linear variable differential transducer (LVDT) with a neat diagram. ***(Nov '23 – 8M, Jul '23 – 6M, Feb '23 – 8M, MQP '22 – 8M)***
10. With a neat diagram, explain the working of LVDT. Also mention the applications of it. ***(Jan '24 – 8M)***
11. A 50 mV output is produced by an LVDT when the core displacement is 10 mm from its zero position. Calculate the core displacement when the output is 35 mV.
12. An LVDT with 0.5 V/mm sensitivity has its output amplified by a factor of 50 and applied to a meter which can display a minimum of 1 mV. Calculate the overall sensitivity of the system, and determine the minimum detectable core displacement.
13. Explain the working principle of capacitive transducer. ***(MQP '22 – 8M)***
14. A parallel plate capacitive transducer has a plate area $(l\ x\ w) = (40mm\ x\ 40mm)$ and plate spacing $\mathrm{d} = 0.5\mathrm{mm}$. Calculate the device capacitance and displacement that causes the capacitance to change by 5 pF. Also determine the transducer sensitivity. ***(Jan '24 – 6M, Nov '23 – 6M, MQP '22 – 5M)***
15. A capacitive transducer is constructed of two half-disc plates. The plates are 2 mm apart, and each has an area of $1.4 \times 10^{-3}\ \mathrm{m}^2$. Calculate the maximum capacitance, and the transducer sensitivity in pF/degree.
16. Write a note on capacitive displacement transducer.
17. Explain the working principle of capacitive pressure transducer. ***(Jul '23 – 6M)***
18. Briefly explain with diagram of a resistance thermometer. ***(Feb '23 – 4M)***
19. The resistance of a coil of nickel wire is 25 Ω at 20 °C. This rises to 37 Ω when the coil has been submerged in a liquid for some time. Calculate the temperature of the liquid.
20. A resistance thermometer has a temperature coefficient of 0.0039 at 20 °C and a resistance of 130 Ω. Calculate the temperature when its resistance measures 175 Ω.
21. Describe a thermistor and sketch approximate resistance/temperature characteristics for a thermistor. ***(Jul '23 – 6M)***

22. Write down the applications of thermal transducer. ***(MQP '22 – 4M)***
23. Write a note on: (i) Thermocouple (ii) Semiconductor temperature sensor
24. Explain the working of a photoconductive cell.
25. Write a short note on photodiodes. ***(Jul '23 – 6M, MQP '22 – 6M)***
26. With a neat diagram explain the operation of a photomultiplier.
27. Write short note on piezoelectric transducer. ***(Nov '23 – 6M)***
28. With neat diagram, explain the operation of a piezoelectric transducer. ***(Feb '23 – 8M, MQP '22 – 6M)***
29. Explain the working principle and applications of piezoelectric transducer. ***(MQP '22 – 8M)***
30. A piezoelectric transducer has plate dimensions of 5 mm $\times$ 4 mm. The crystal material has a 3 mm thickness and a relative permittivity of 800. The voltage sensitivity is 0.04 Vm/N. Calculate the transducer charge sensitivity, the charge, and the output voltage when the applied force is 8 N.
31. A piezoelectric transducer has plate dimensions of 5 mm ×4 mm. The crystal material has a 3 mm thickness and a relative permittivity of 800. The voltage sensitivity is 0.04 Vm/N. Calculate the transducer charge sensitivity, the charge, and the output voltage when the applied force is 8 N.

Communications

1. With a neat block diagram, explain the simple communication system. ***(Jan '24 – 6M)***
2. Explain the various blocks involved in an electrical communication system. ***(Nov '23 – 6M, MQP '22 – 6M)***
3. Explain the various blocks involved in communication block diagram. ***(Feb '23 – 8M)***
4. Describe the blocks of the basic communication system. ***(MQP '22 – 7M)***
5. With neat block diagram, explain the working of communication system. ***(Jul '23 – 8M)***
6. Explain typical radio transmitter with neat block diagram. ***(MQP '22 – 6M)***
7. What is noise? Explain the term Channel Noise and its effects. ***(MQP '22 – 6M)***
8. With a neat block diagram, explain AM superheterodyne receiver. ***(Jan '24 – 6M)***
9. Describe with diagram of an AM superheterodyne receiver, explain each block. ***(Feb '23 – 8M)***
10. What is modulation? Explain the need for modulation in communication system. ***(Nov '23 – 6M, Jul '23 – 8M, MQP '22 – 8M, 7M, 6M)***