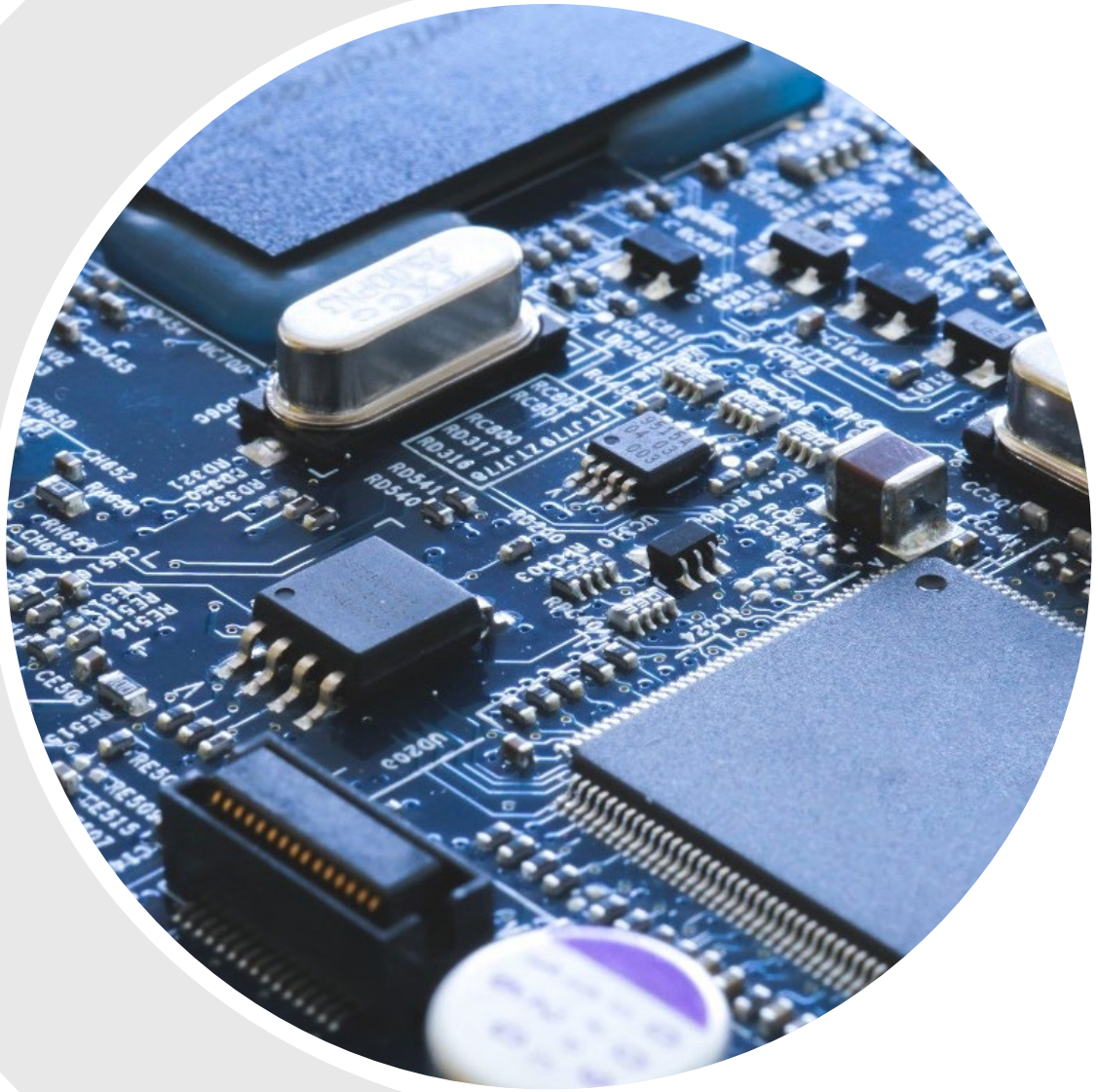

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BASIC ELECTRONICS

(BBEE103/BBEE203)

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MODULE – 2

Field Effect Transistors

Introduction

Field Effect Transistor

- The Field-Effect Transistor (FET) is a three-terminal device that uses electric field to control the current flowing through the device.
- It has three terminals – Source (S), Drain (D) and Gate (G).
- FETs are unipolar devices because they operate only with one type of charge carrier.
- The term *field-effect* relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminals (gate).

Field Effect Transistor

- An FET is a voltage-controlled device, where the voltage between two of the terminals (gate and source) controls the current through the device.
- Unlike a BJT, an FET requires virtually no input current.
  - This gives it an extremely high input resistance, which is its major advantage over BJT.
- Because of their nonlinear characteristics, they are generally not as widely used in amplifiers as BJTs, except where very high input impedances are required.
- However, FETs are the preferred device in low-voltage switching applications because they are generally faster than BJTs when turned on and off.

Field Effect Transistor

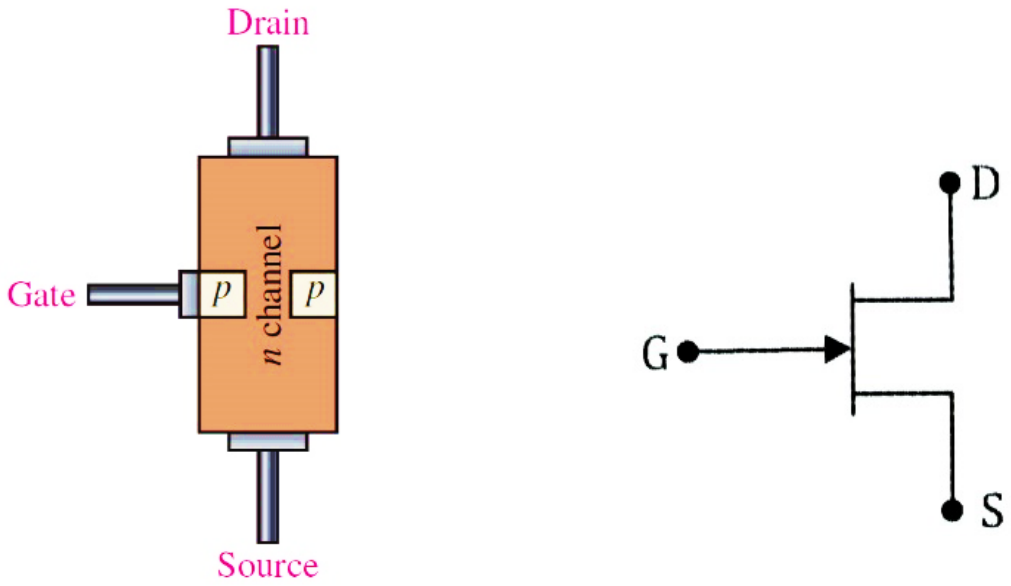
- The two main categories of FETs are:
  - Junction Field-Effect Transistor (JFET)
  - Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)

Junction Field-Effect Transistor (JFET)

JFET

- The JFET (Junction Field-Effect Transistor) is a type of FET that operates with a reverse-biased pn-junction to control current in a channel.
- Depending on their structure, JFETs are classified into two types:
  - N-channel JFET
  - P-channel JFET

N-Channel JFET



(a) Basic structure (b) Symbol

Fig. 1 N-channel JFET

N-Channel JFET

- A piece of *n*-type semiconductor material, referred to as *channel*, is sandwiched between two smaller pieces of *p*-type (*gates*).
- The ends of the channel are designated as the *drain (D)* and the *source (S)*.
- The two pieces of *p*-type material are connected together and their terminal is named the *gate (G)*.

N-Channel JFET

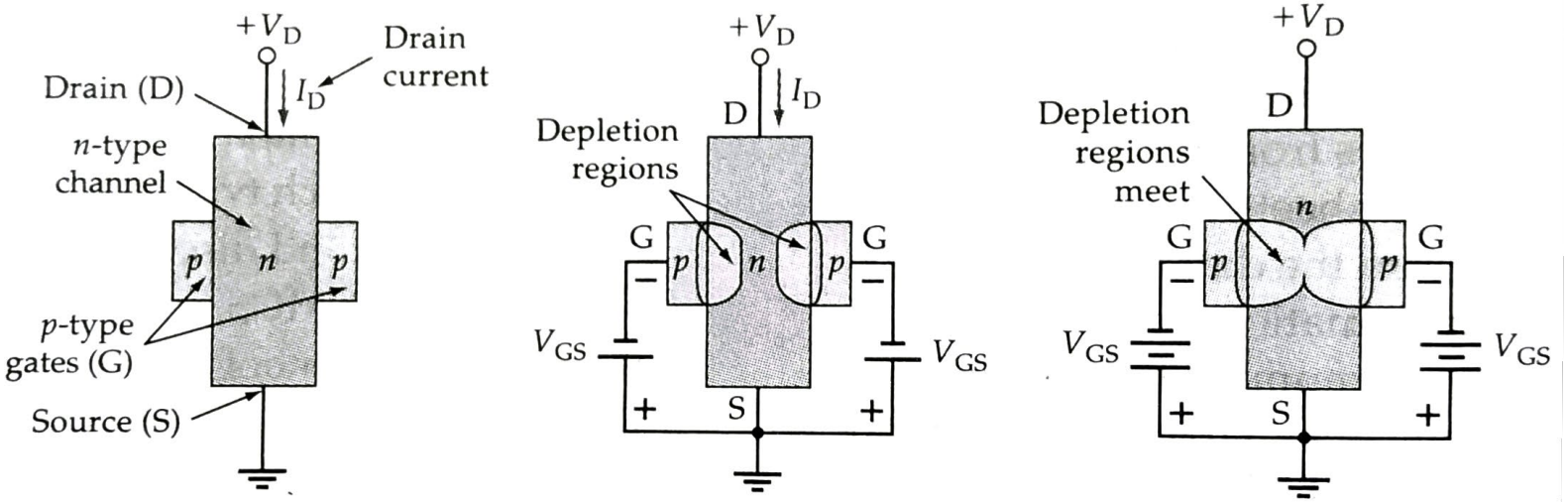


Figure 9-1 An *n*-channel JFET consists of an *n*-type channel with *p*-type gate regions on each side.

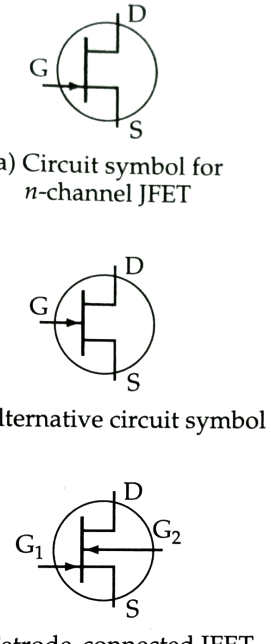


Figure 9-2 Circuit symbols for an *n*-channel JFET. Like all semiconductor symbols, the arrowheads point from the *p*-type to the *n*-type material.

N-Channel JFET

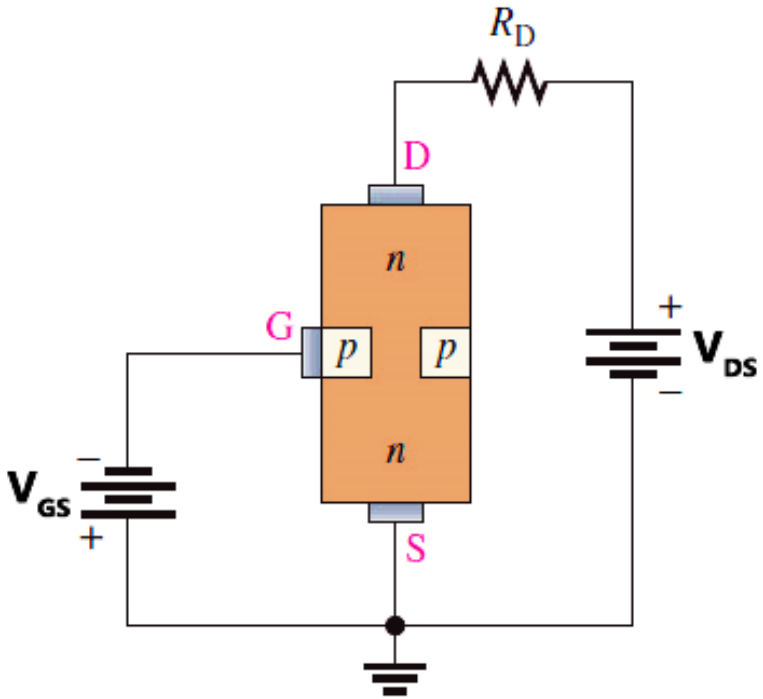


Fig. 2 A biased N-channel JFET

Note:

In an n-channel JFET, V_{GS} is negative and V_{DS} is positive.

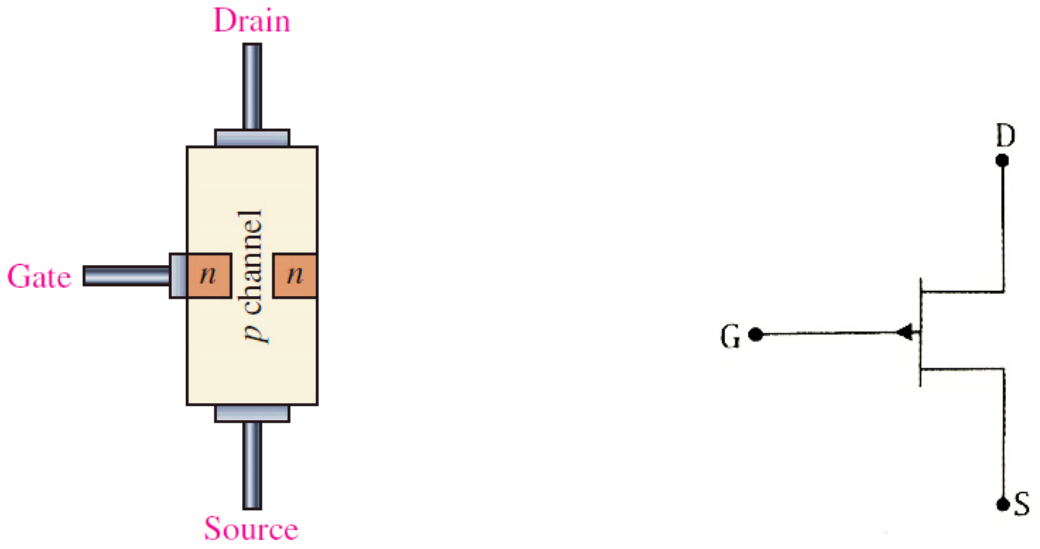
N-Channel JFET

- With the gate left unconnected and a drain-source voltage V_D applied (positive at the drain, negative at the source), a drain current I_D flows as shown.
- When a gate-source voltage V_{GS} is applied with the gate negative with respect to the source, the gate-channel *pn*-junctions are reverse biased.
- The channel is more lightly doped than the gate material, so the depletion regions penetrate deep into the channel.
- Since depletion regions do not have charge carriers, they behave as insulators.
- As a result, the channel becomes narrow, its resistance increases, and I_D reduces.
- When the negative gate-source bias voltage is further increased, the depletion regions meet at the centre of the channel and I_D is cut off.

N-Channel JFET

- An ac signal applied to the gate causes the reverse gate-source voltage to increase as the instantaneous level of the signal goes negative, and to decrease when the signal goes positive.
- When the signal goes negative, the depletion regions widen, the channel resistance is increased and the drain current decreases.
- When the signal goes positive, the depletion regions recede, the channel resistance is reduced and the drain current increases.

P-Channel JFET



(a) Basic structure (b) Symbol

Fig. 3 P-channel JFET

P-Channel JFET

- In a p-channel JFET, the channel is a p-type semiconductor, and the gates are n-type.
- The drain-source voltage V_D is applied negative to the drain and positive to the source.
- The drain current I_D flows from source to drain.
- The bias voltage is applied positive on the gate and negative on the source.
  - So the gate-channel junctions are reverse biased.

P-Channel JFET

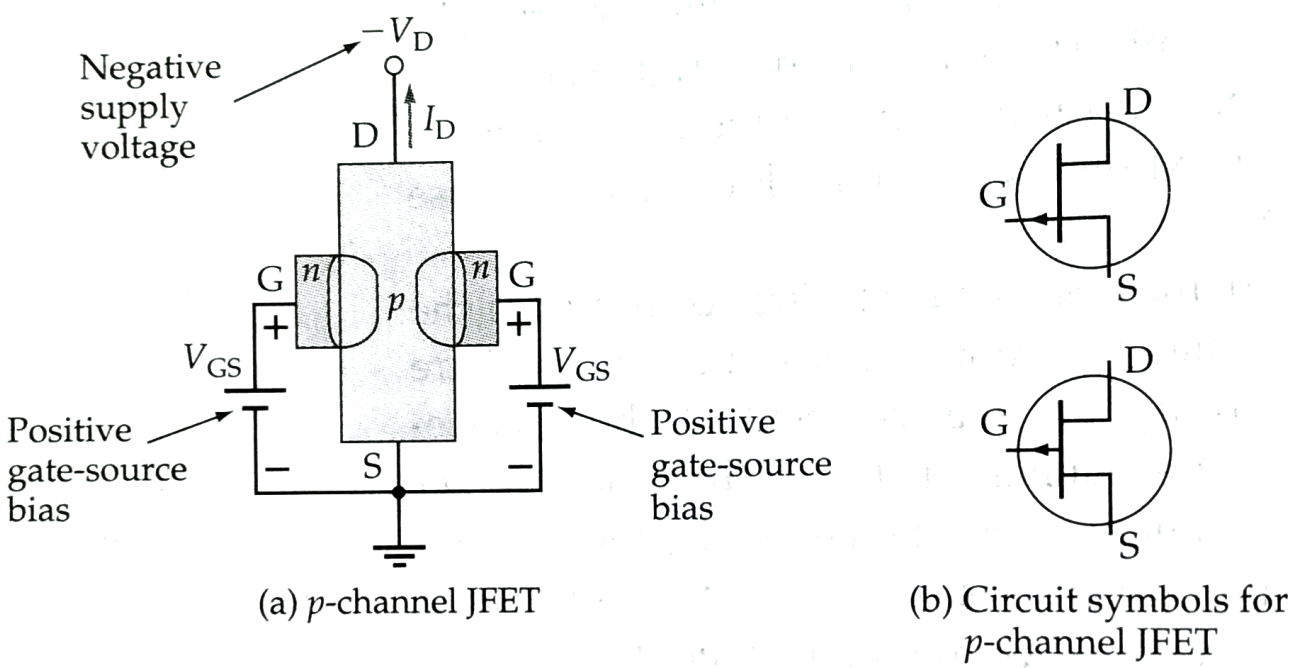


Figure 9-3 A *p*-channel JFET operates in exactly the same way as an *n*-channel device, except that the current directions and voltage polarities are reversed.

P-Channel JFET

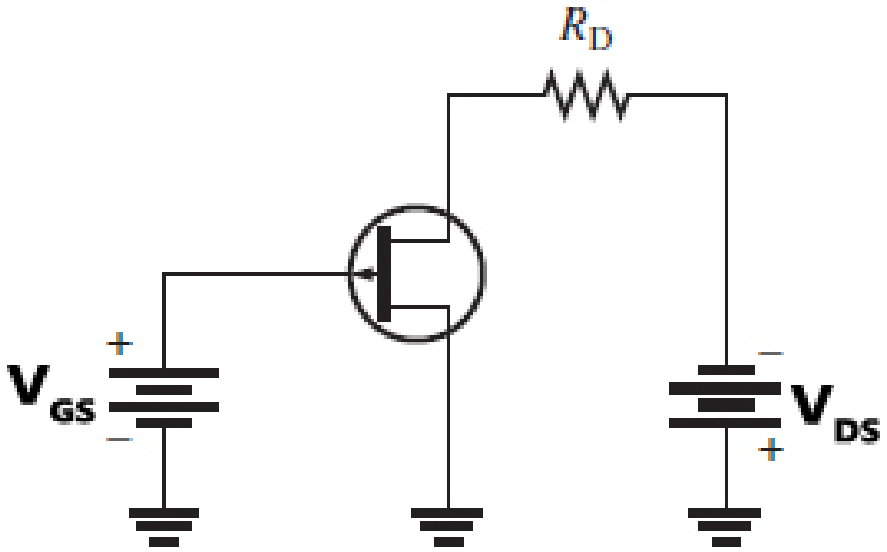


Fig. 4 A biased P-channel JFET

Note:

In an p-channel JFET, V_{GS} is positive and V_{DS} is negative.

P-Channel JFET

- In a p-channel JFET, the channel is a p-type semiconductor, and the gates are n-type.
- The drain-source voltage V_D is applied negative to the drain and positive to the source.
- The drain current I_D flows from source to drain.
- The bias voltage is applied positive on the gate and negative on the source.
  - So the gate-channel junctions are reverse biased.

JFET Fabrication and Packaging

- JFETs are normally manufactured by the diffusion process.
- For an *n*-channel JFET, starting with a *p*-type substrate, an *n*-channel is diffused; then *p*-type impurities are diffused into the channel.
- Finally, metal terminal connections are deposited through holes in the silicon dioxide surface.
- The *n*-type region is the FET channel, and the two *p*-type regions constitute the gates.

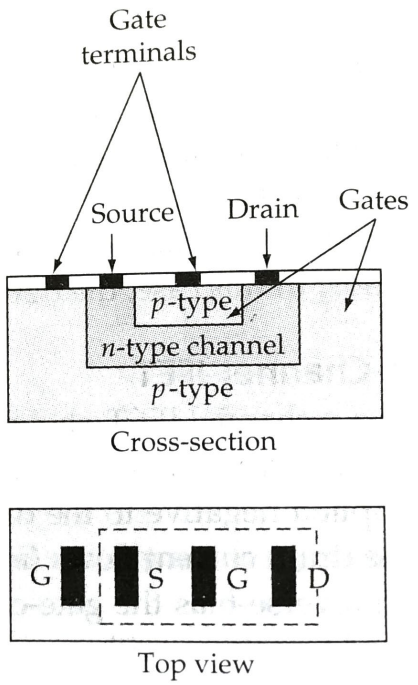
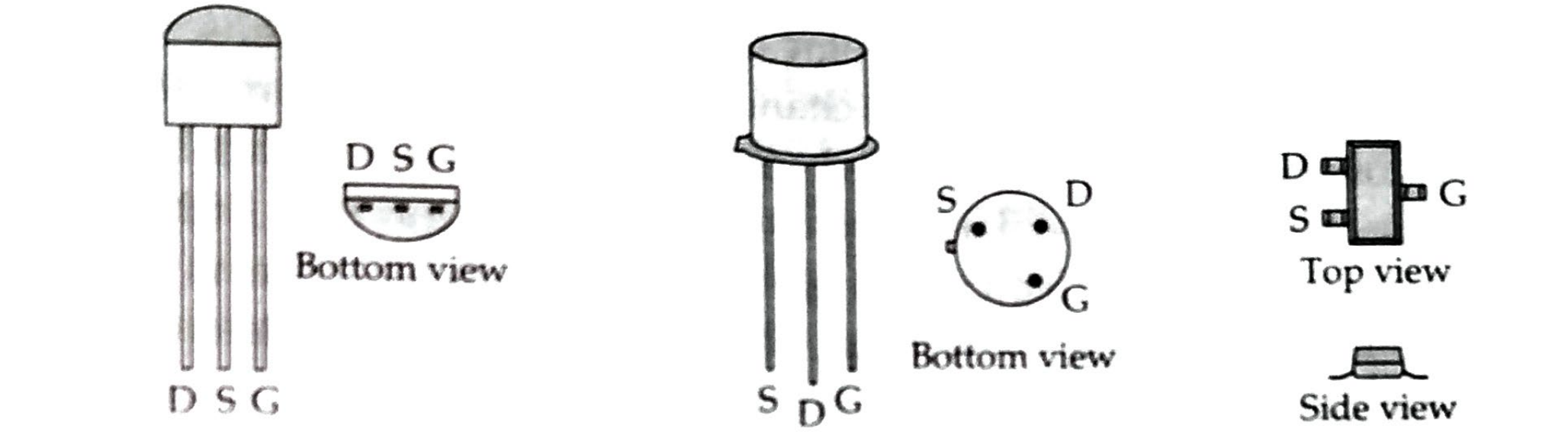


Figure 9-4 Cross-section and top view of *n*-channel JFET. With this type of construction, the drain and source are interchangeable.

JFET Fabrication and Packaging



(a) Resin encapsuled FET (b) Metal can-enclosed FET (c) Surface mount FET

Figure 9-5 Various JFET enclosures.

JFET Characteristics

Characteristics of N-Channel JFET

- Drain Characteristics
  - It is the plot of V_{DS} vs I_D for constant values of V_{GS}.
- Transfer Characteristics
  - It is the plot of V_{GS} vs I_D for constant values of V_{DS}.

Drain Characteristics of N-Channel JFET

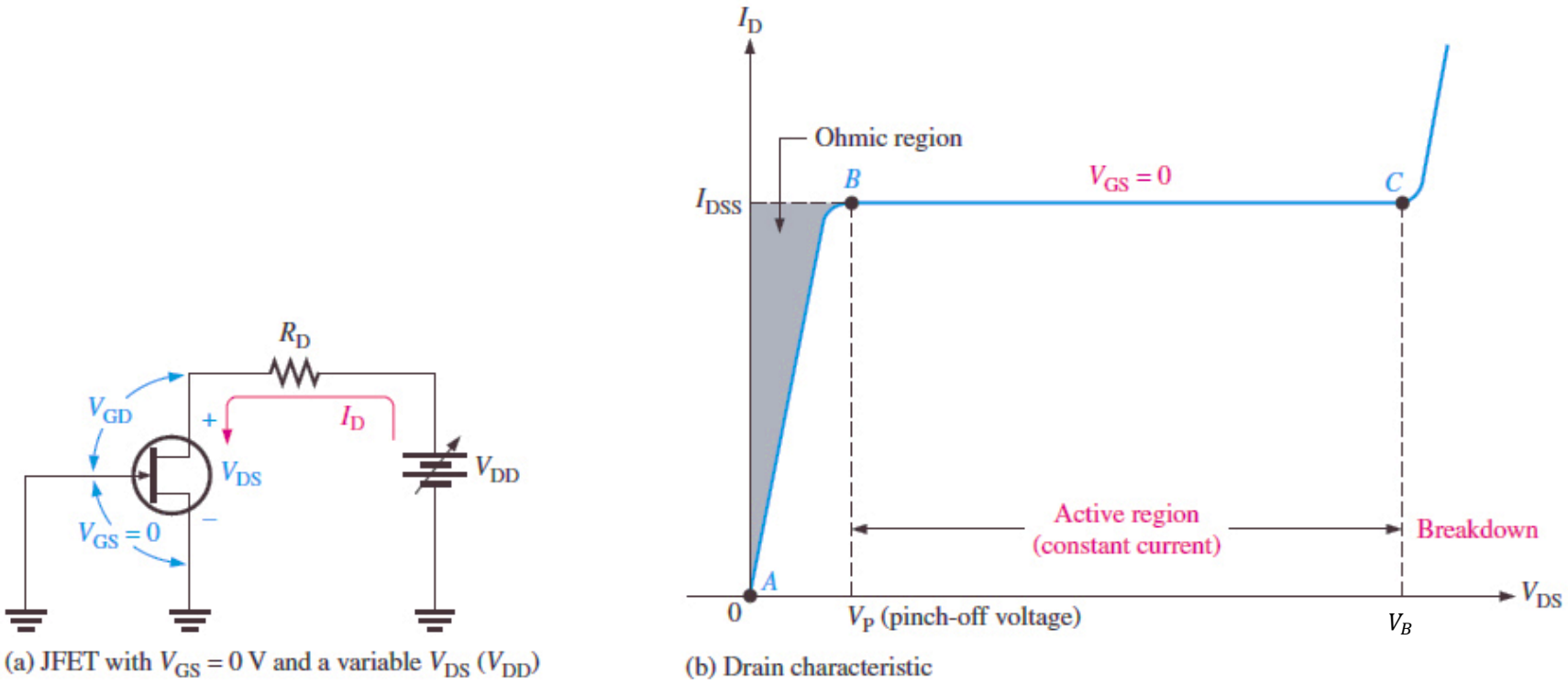


Fig. 5 Drain characteristic of N-channel JFET for $V_{GS} = 0$

Drain Characteristics of N-Channel JFET

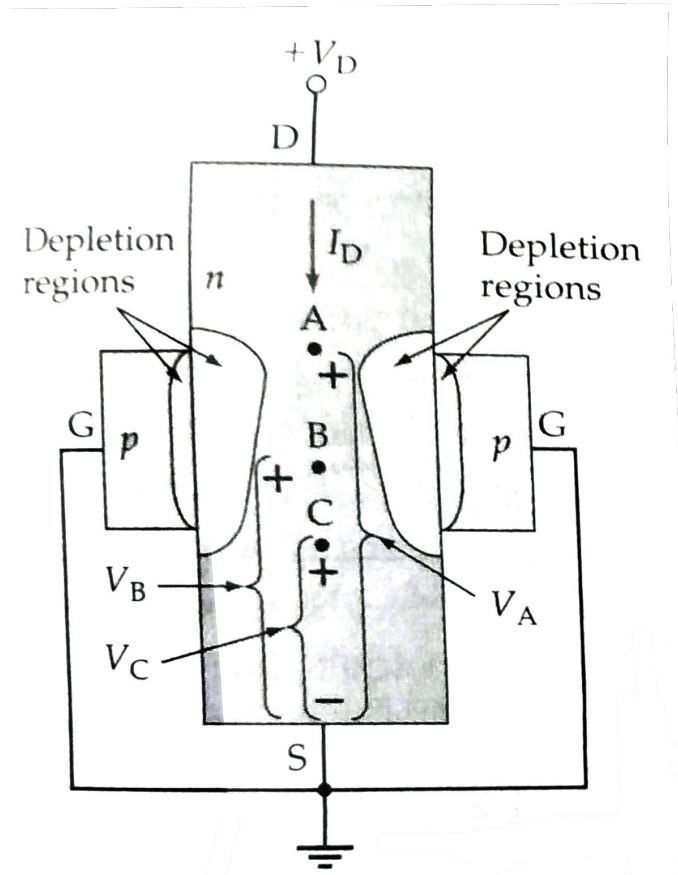


Figure 9-6 Drain current in an *n*-channel JFET causes voltage drops along the channel which reverse-bias the gate channel junctions. This produces different levels of depletion region penetration into the channel.

Drain Characteristics of N-Channel JFET

- Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0\ V$) as shown in Fig. 5 (a).
- As V_{DD} (and thus V_{DS}) is increased from 0 V, I_D will increase proportionally, as shown in the graph of Fig. 5 (b) between points A and B.
- In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect.
- This is called the *ohmic region* because V_{DS} and I_D are related by Ohm's law.

Drain Characteristics of N-Channel JFET

- At point B in Fig. 5 (b), the curve levels off and enters the active region where I_D becomes constant.
- As V_{DS} increases from point B to point C, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

Drain Characteristics of N-Channel JFET

- **Pinch-off Voltage (V_P):**
  - It is the value of V_{DS} at which I_D becomes constant for $V_{GS} = 0\ V$ (point B on the curve in Fig. 5 (b)).
  - For a given JFET, V_P has a fixed value.
- A continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current.
  - This value of drain current is $\boldsymbol{I_{DSS}}$ **(Drain-Source Saturation Current).**
  - $\boldsymbol{I_{DSS}}$ is the maximum drain current that a specific JFET can produce when the gate is shorted, i.e., $V_{GS} = 0\ V$.

Drain Characteristics of N-Channel JFET

- **Breakdown:**
  - When V_{DS} exceeds the breakdown voltage V_B (point C in Fig. 5 (b)), breakdown occurs and I_D begins to increase very rapidly with any further increase in V_{DS}.
  - Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points B and C on the graph).

Drain Characteristics of N-Channel JFET

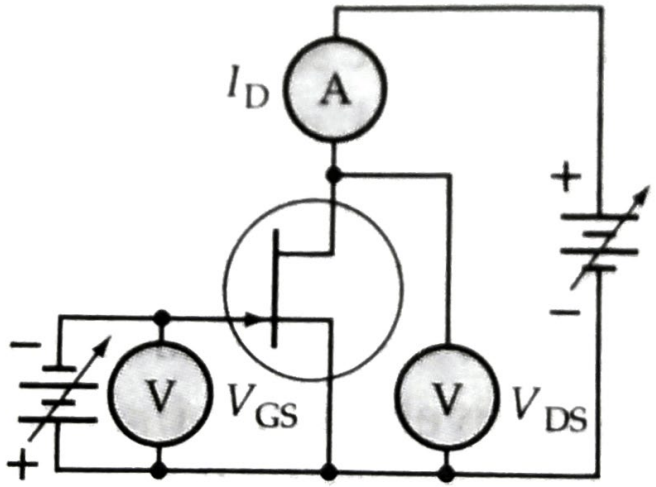


Figure 9-9 Circuit for obtaining the I_D/V_{DS} characteristic for an *n*-channel junction field effect transistor with various gate-source bias voltages.

Drain Characteristics of N-Channel JFET

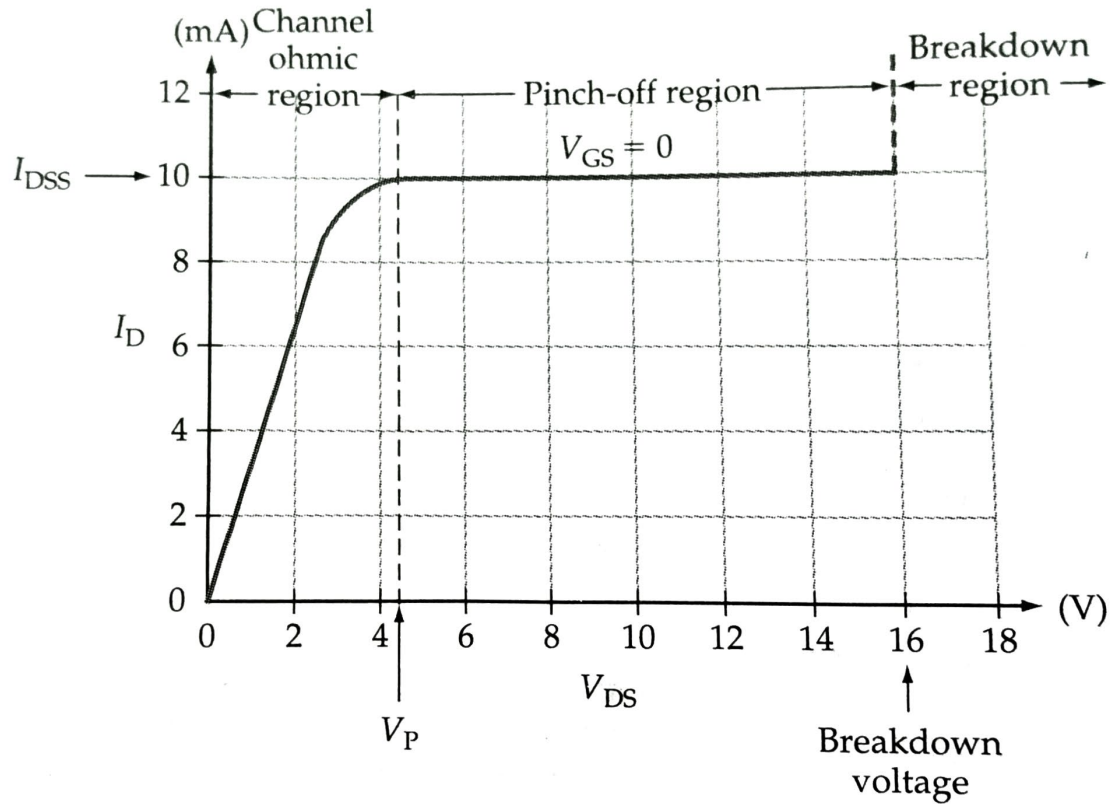


Figure 9-8 I_D/V_{DS} characteristic for an *n*-channel JFET with $V_{GS} = 0$.

Drain Characteristics of N-Channel JFET

- Fig. 6 shows drain characteristics of N-channel for different values of V_{GS}.

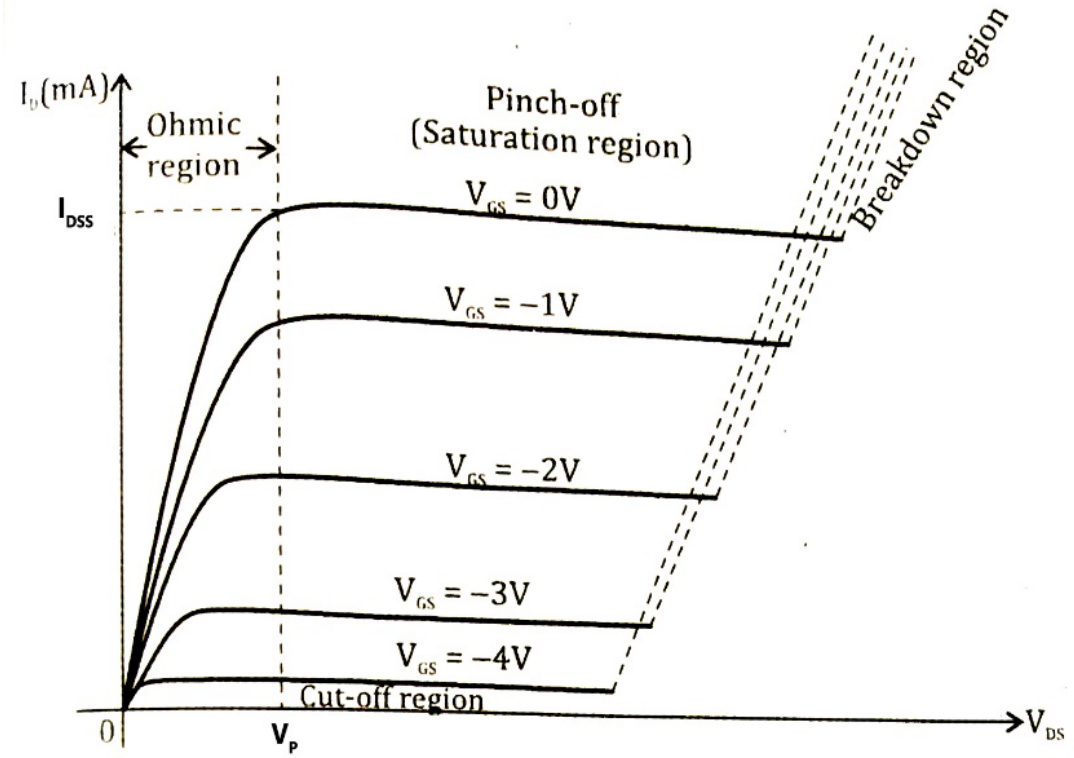


Fig. 6 Drain characteristic of N-channel JFET

Drain Characteristics of N-Channel JFET

- The different regions on the JFET drain characteristics are summarized as below:
  i. **Ohmic Region:** In this region, the channel of JFET obeys Ohm's law.
  ii. **Pinch-off Region/Saturation Region:** In this region, I_D is maximum and remains constant for a given V_{GS}.
  iii. **Breakdown Region:** In this region, the *pn*-junction breaks down and I_D increases abruptly. The JFET loses its ability to control I_D.
  iv. **Cut-off Region:** In this region, JFET if OFF, i.e., $I_D = 0$.

Transfer Characteristics of N-Channel JFET

- Fig. 7 shows the transfer characteristic curve for an N-channel JFET.
  - This curve is also known as a transconductance curve.

Note:

In an N-channel JFET, V_{GS} is negative and V_{DS} is positive.

$V_{GS(off)}$ is negative.

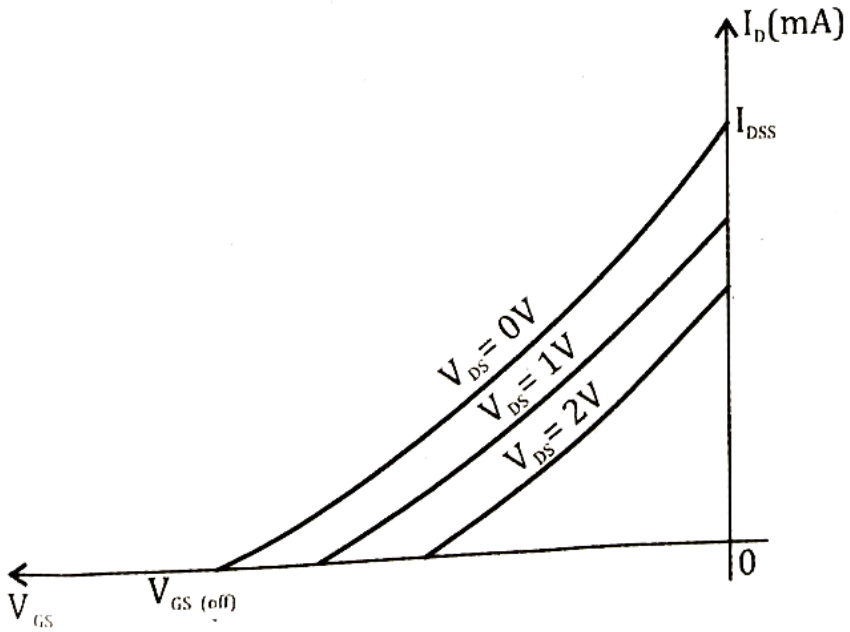


Fig. 7 Transfer characteristic of N-channel JFET

Transfer Characteristics of N-Channel JFET

- As observed, a range of V_{GS} values from 0 to $V_{GS(off)}$ controls the amount of drain current.
- $V_{GS(off)}$ is called the *cut-off voltage*.
- **Cut-off Voltage ($V_{GS(off)}$):**
  - It is the value of V_{GS} that makes I_D approximately zero.
  - The cut-off voltage $V_{GS(off)}$ and pinch-off voltage V_P are always equal in magnitude but opposite in sign, i.e., $V_{GS(off)} = -V_P$.
  - $V_{GS(off)}$ is negative for an N-channel JFET and positive for a P-channel JFET.

Transfer Characteristics of N-Channel JFET

- Fig. 8 is a general (universal) transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D.

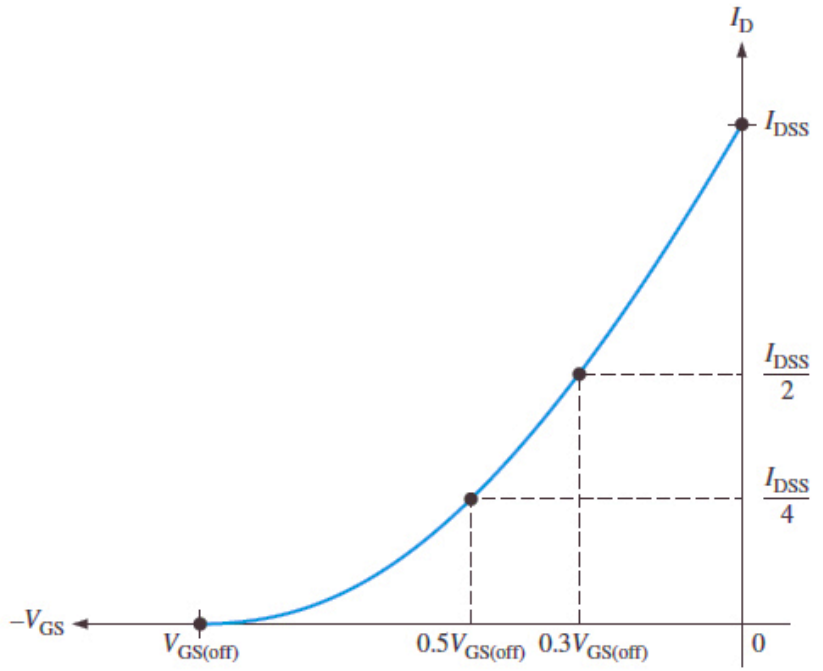


Fig. 8 N-channel JFET universal transfer characteristic curve

Characteristics of P-Channel JFET

- Drain Characteristics
  - It is the plot of V_{DS} vs I_D for constant values of V_{GS}.
- Transfer Characteristics
  - It is the plot of V_{GS} vs I_D for constant values of V_{DS}.

Characteristics of P-Channel JFET

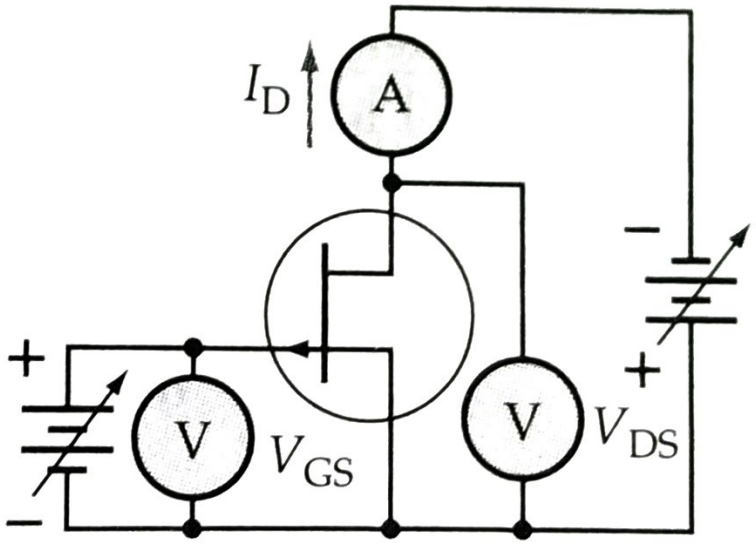


Figure 9-15 Circuit for determining the characteristics of a *p*-channel JFET.

Drain Characteristics of P-Channel JFET

- Fig. 9 shows the drain characteristics of a P-channel JFET.

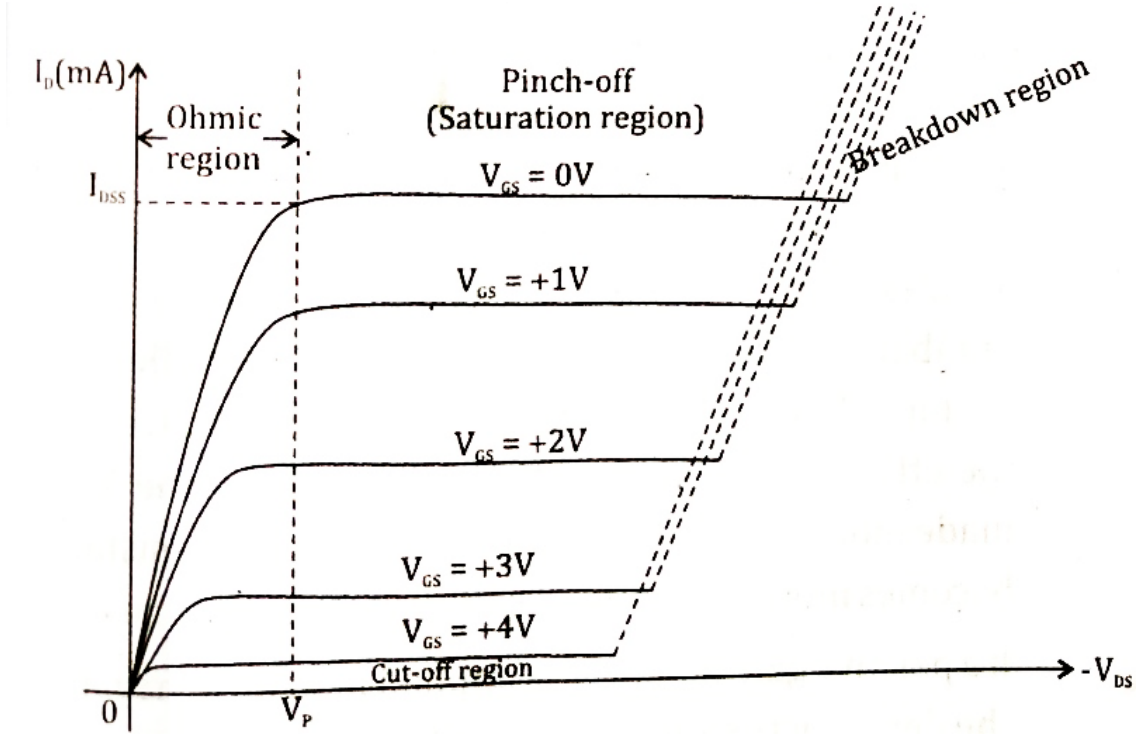


Fig. 9 Drain characteristics of P-channel JFET

Transfer Characteristics of P-Channel JFET

- Fig. 10 shows the transfer characteristics of a P-channel JFET.

Note:

In a P-channel JFET, V_{GS} is positive and V_{DS} is negative.

$V_{GS(off)}$ is positive.

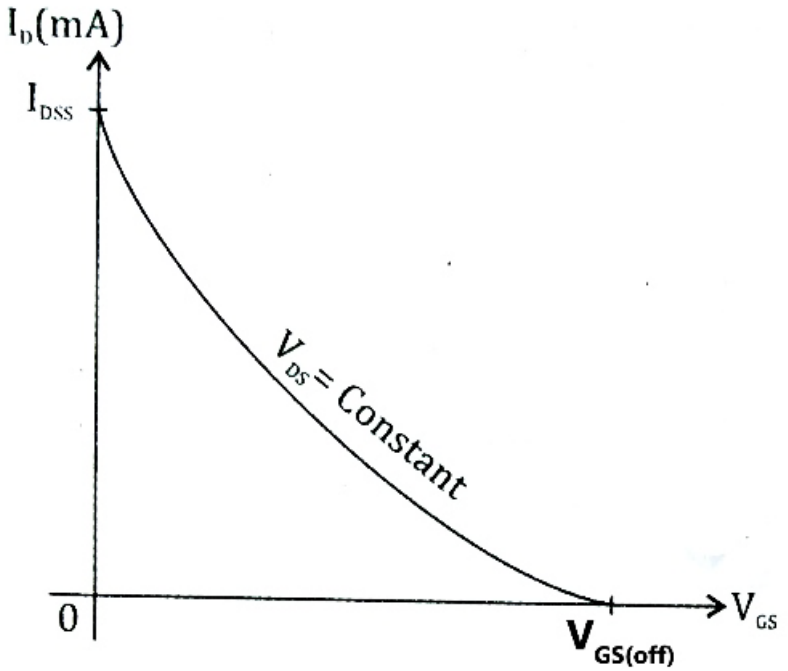


Fig. 10 Transfer characteristics of P-channel JFET

Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)

MOSFET

- The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) is a type of FET which has no *pn*-junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer.
- The two basic types of MOSFETs are Enhancement type (E-MOSFET) and Depletion type (D-MOSFET).
  - Of the two types, the Enhancement MOSFET is more widely used.
- Because polycrystalline silicon is now used for the gate material instead of metal, MOSFETs are sometimes called IGFETs (Insulated-Gate FETs).

MOSFET (continued)

- The MOSFET has two modes of operation – enhancement mode and depletion mode.
  - An E-MOSFET can be operated only in enhancement mode and has no depletion mode.
  - A D-MOSFET can be operated in either depletion mode or enhancement mode and hence it is also called depletion-enhancement MOSFET.

Enhancement MOSFET (E-MOSFET)

- An E-MOSFET can be operated only in enhancement mode and has no depletion mode.
- An E-MOSFET has no structural channel.
- It is also called EMOS Transistor.
- The basic structure of an N-channel E-MOSFET is shown in Fig. 11 (a).

Enhancement MOSFET (E-MOSFET)

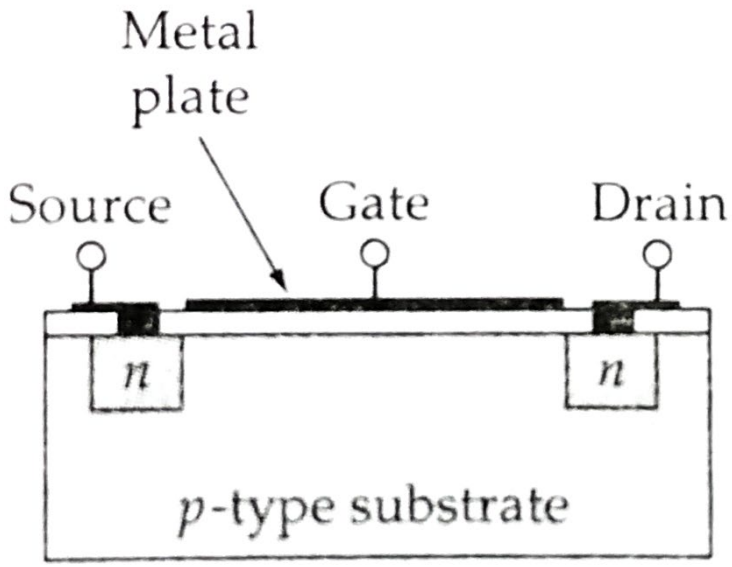


Figure 9-29 Metal oxide semiconductor FET (MOS-FET) construction.

Enhancement MOSFET (E-MOSFET)

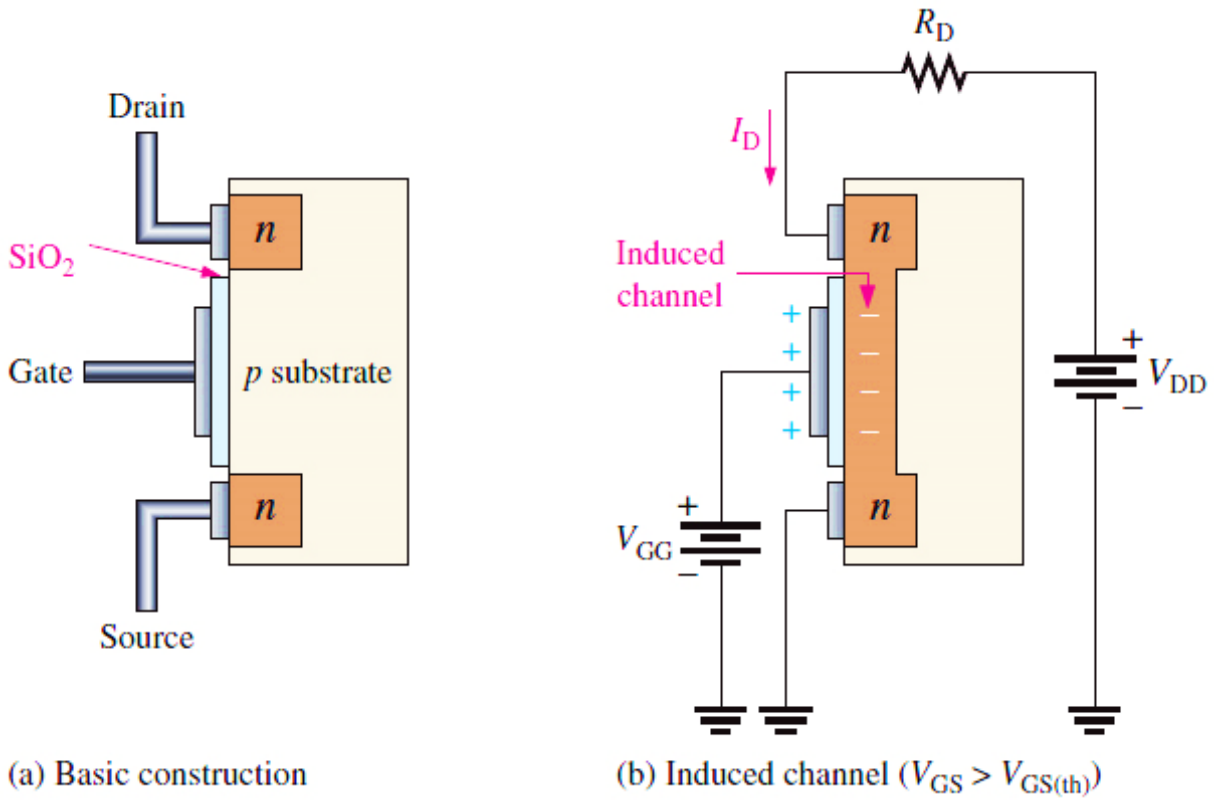


Fig. 11 Construction and operation of N-channel E-MOSFET

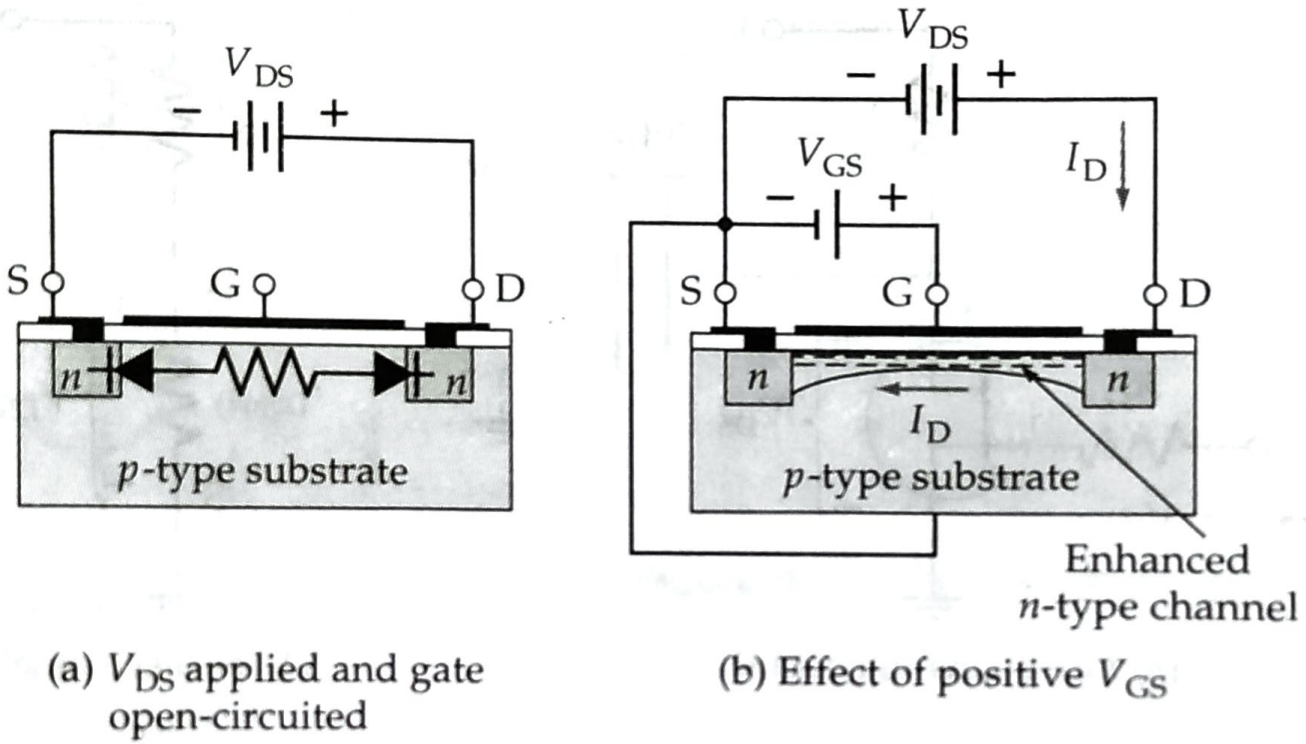
Enhancement MOSFET (E-MOSFET)

- A *p*-type substrate is the basic structure upon which *n*-type regions are created by diffusion.
- An oxide (SiO_2) layer which acts as an insulator covers the entire *p*-type substrate and *n*-type regions.
- By etching proper openings through the oxide layer, metal contacts for source and drain connections are made to the *n*-regions.
- The gate contact is formed on the surface of the oxide layer.
- The gate is electrically insulated from both *n*-type regions and the *p*-type substrate.

Enhancement MOSFET (E-MOSFET)

- Regardless of the polarity of applied voltage, no electrons can flow from source to drain because the *n*-type source, *p*-type substrate and *n*-type drain behave as two *pn*-junctions connected back-to-back and one of the *pn*-junctions is always reverse biased.

Enhancement MOSFET (E-MOSFET)



(a) V_{DS} applied and gate open-circuited

(b) Effect of positive V_{GS}

Figure 9-30 Effect of $+V_{DS}$ on the MOSFET with the gate terminal open-circuited and with $+V_{GS}$ applied to the gate.

Enhancement MOSFET (E-MOSFET)

- Consider a positive voltage is applied between gate and source as shown in Fig. 11 (b).
- As the oxide layer is an insulator sandwiched between two conductive regions, a capacitive effect is formed.
- The metal surface which is gate and the conducting substrate act as the capacitor plates.
- When a positive charge is applied to one plate of the capacitor, a corresponding negative charge is induced on the opposite plate due to the electric field between the plates.
- In this case, the positive potential at the gate induces negative charges in the p-type substrate.

Enhancement MOSFET (E-MOSFET)

- This charge results from minority carriers (electrons) attracted towards the area of the gate.
- As the number of electrons reaching the region increases, the N-channel is formed gradually and resistance between source and drain decreases.
- The greater the gate potential, the lower the channel resistance and higher the drain current I_D.
- This process is called *enhancement* and the resulting device is called *enhancement* type MOSFET (E-MOSFET).

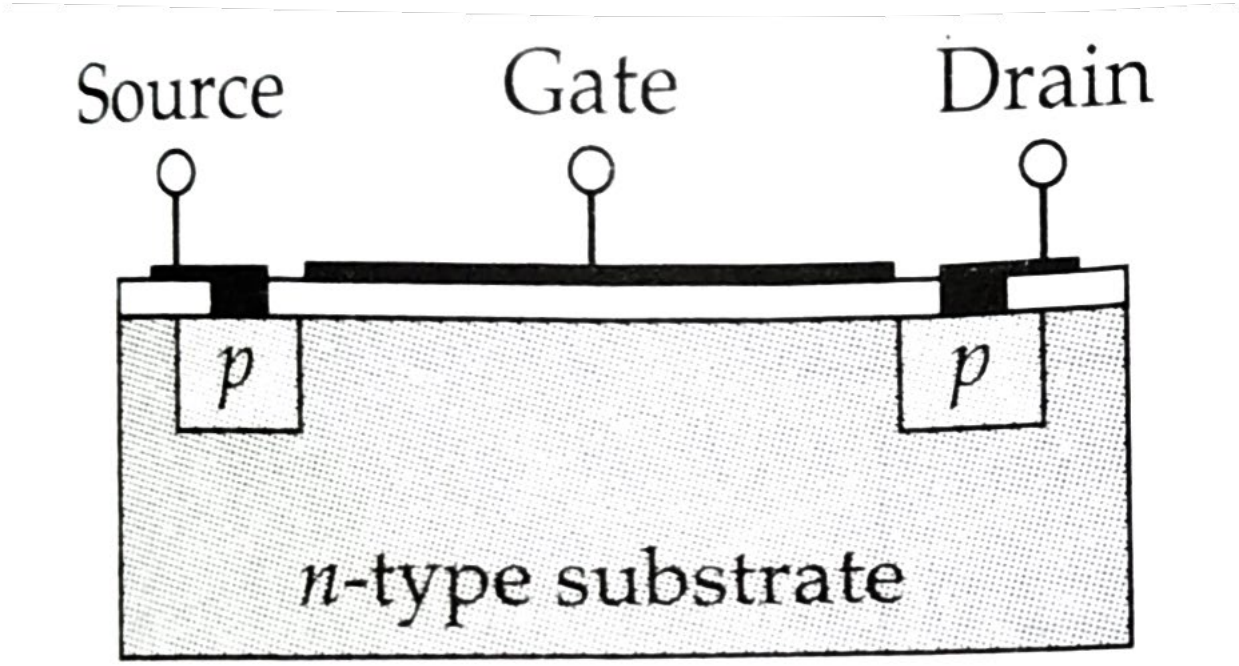
Enhancement MOSFET (E-MOSFET)

- Fig. 12 shows the symbols of N-channel and P-channel E-MOSFET.

(a) N-channel E-MOSFET (b) P-channel E-MOSFET

Fig. 12 Symbols of E-MOSFET

Enhancement MOSFET (E-MOSFET)



(a) *p*-channel EMOSFET

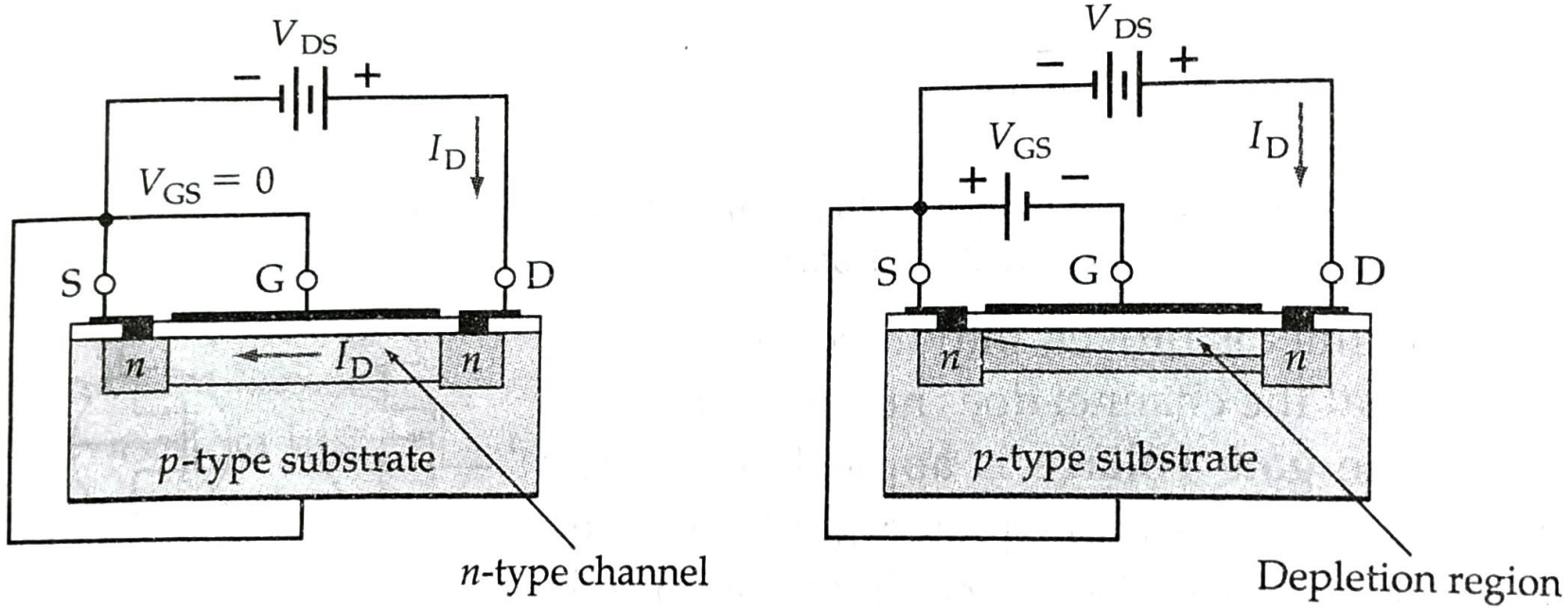
Enhancement MOSFET (E-MOSFET)

- In a P-channel E-MOSFET, the substrate is of *n*-type and the diffused regions are of *p*-type.
- When a negative voltage is applied between the gate and source, a P-channel is induced in the *n*-type substrate.
- The operation of P-channel E-MOSFET can be explained on the same grounds as of N-channel, except the voltage polarities are opposite to those of the N-channel.

Depletion-Enhancement MOSFET (D-MOSFET)

- A D-MOSFET can be operated in either depletion mode or enhancement mode and hence it is also called depletion/enhancement MOSFET.
- It is also called DMOS Transistor.
- Fig. 13 shows the basic structure of N-channel and P-channel D-MOSFETs.

Depletion-Enhancement MOSFET (D-MOSFET)



(a) I_D flows even when $V_{GS} = 0$

(b) I_D decreases when V_{GS} is negative, and increases when V_{GS} is positive

Figure 9-34 *n*-Channel depletion-enhancement MOSFET.

Depletion-Enhancement MOSFET (D-MOSFET)

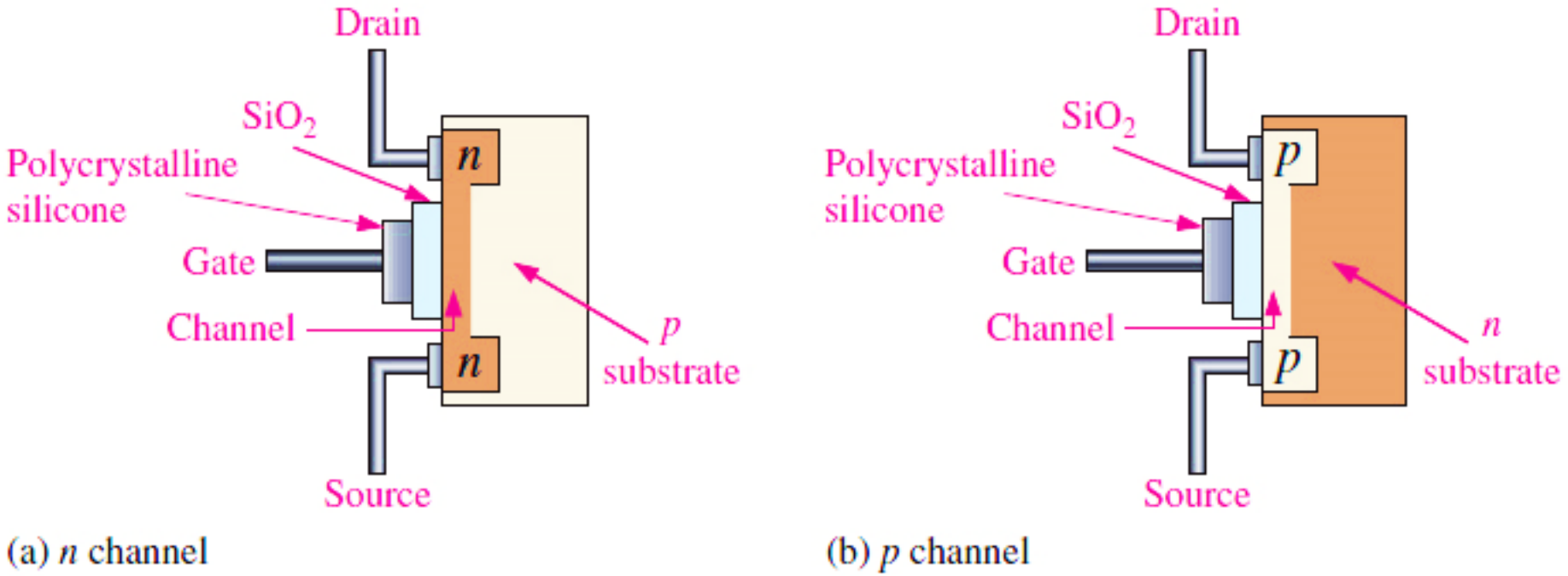


Fig. 13 Basic structure of D-MOSFETs

Depletion-Enhancement MOSFET (D-MOSFET)

- The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate.
- In an N-channel D-MOSFET, the substrate is of *p*-type and the diffused regions are of *n*-type and the channel is formed by doping *n*-type material adjacent to the gate.
- In a P-channel D-MOSFET, the substrate is of *n*-type and the diffused regions are of *p*-type and the channel is formed by doping *p*-type material adjacent to the gate.

Depletion-Enhancement MOSFET (D-MOSFET)

- Consider a N-channel D-MOSFET.
- Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied.
- The N-channel D-MOSFET operates in the depletion mode when a negative gate-to-source voltage is applied and in the enhancement mode when a positive gate-to-source voltage is applied.
- D-MOSFETs are generally operated in the depletion mode.

Depletion-Enhancement MOSFET (D-MOSFET)

Depletion Mode

- When a negative voltage is applied between the gate and source, the negative charges on the gate induce an equal amount of positive charges (holes) on the other side of the oxide layer.
- This results in the recombination of holes with electrons in the channel and reduces the number of free electrons available.
- This makes the channel depleted of charge carriers which increases the effective resistance of the channel.
- As the V_{GS} is made more and more negative, the channel resistance becomes more and more, resulting in lesser drain current.
- At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero.

Depletion-Enhancement MOSFET (D-MOSFET)

Enhancement Mode

- When a positive voltage is applied between the gate and source, free electrons are induced in the N-channel, which enhances the channel conductivity and thus I_D increases.

Depletion-Enhancement MOSFET (D-MOSFET)

- Fig. 14 shows the symbols of N-channel and P-channel D-MOSFET.

(a) N-channel D-MOSFET (b) P-channel D-MOSFET

Fig. 14 Symbols of D-MOSFET

Depletion-Enhancement MOSFET (D-MOSFET)

- The operation of P-channel D-MOSFET can be explained on the same grounds as of N-channel, except the voltage polarities are opposite to those of the N-channel.

MOSFET Characteristics and Parameters

MOSFET Characteristics

- Drain Characteristics
  - It is the plot of V_{DS} vs I_D for constant values of V_{GS}.
- Transfer Characteristics
  - It is the plot of V_{GS} vs I_D for constant values of V_{DS}.

E-MOSFET Drain Characteristics

- Fig. 15 shows the drain characteristics of an N-channel E-MOSFET.

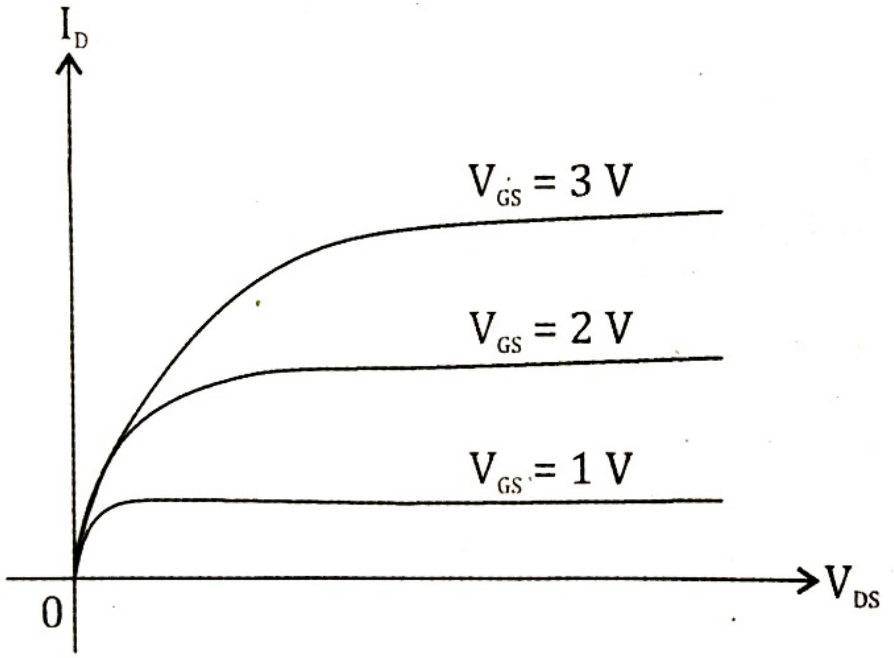


Fig. 15 Drain characteristics of N-channel E-MOSFET

E-MOSFET Drain Characteristics

- The drain characteristics of P-channel E-MOSFET is similar to that N-channel, but in P-channel, V_{DS} and V_{GS} are negative.

D-MOSFET Drain Characteristics

- Fig. 16 shows the drain characteristics of an N-channel D-MOSFET.
- The N-channel D-MOSFET is in depletion mode when V_{GS} is negative and in enhancement mode when V_{GS} is positive.
-

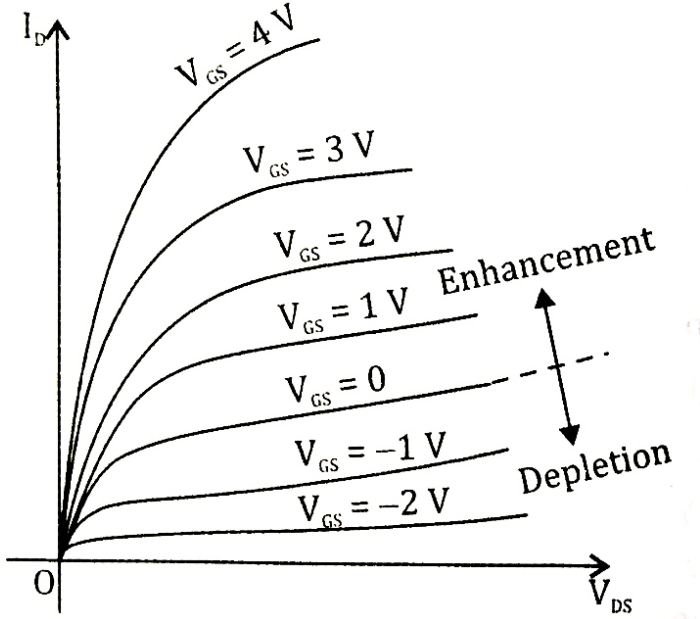


Fig. 16 Drain characteristics of N-channel D-MOSFET

D-MOSFET Drain Characteristics

- The P-channel D-MOSFET is in depletion mode when V_{GS} is positive and in enhancement mode when V_{GS} is negative.

E-MOSFET Transfer Characteristics

- Fig. 17 shows the transfer characteristics of N-channel and P-channel E-MOSFETs.

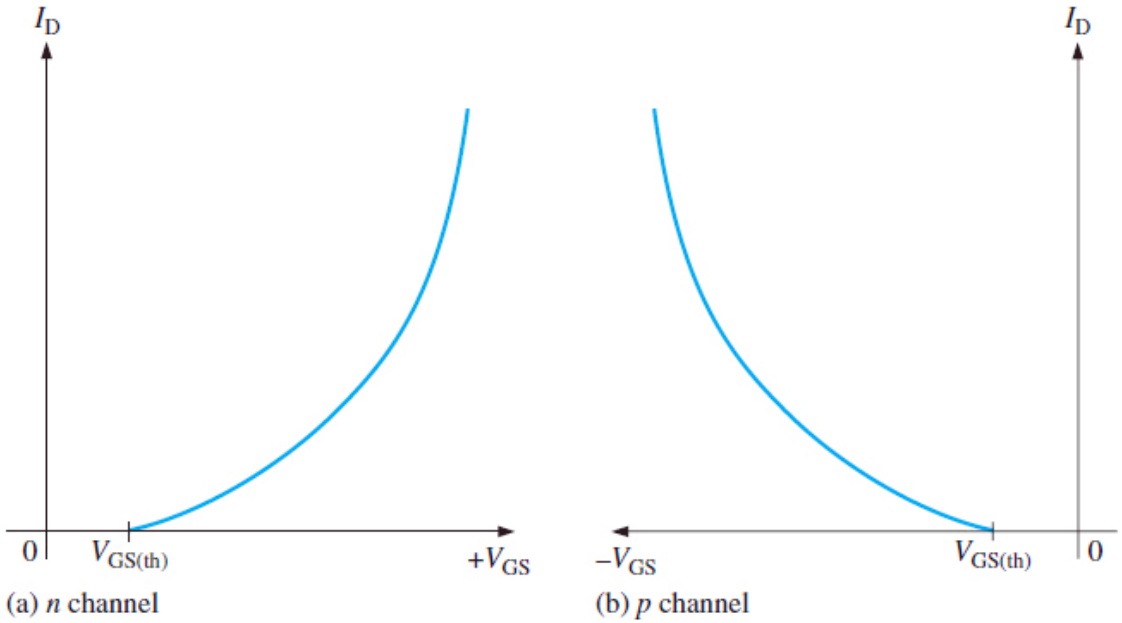


Fig. 17 General transfer characteristics of E-MOSFET

E-MOSFET Transfer Characteristics

- The E-MOSFET uses only channel enhancement.
  - Therefore, an N-channel device requires a positive V_{GS}, and a P-channel device requires a negative V_{GS}.
- From the characteristic, there is no drain current when $V_{GS} = 0$.
  - Therefore, the E-MOSFET does not have a significant I_{DSS} parameter.
- Also, there is ideally no drain current until V_{GS} reaches a certain nonzero value called the threshold voltage, $V_{GS(th)}$.
- **Threshold voltage $V_{GS(th)}$:**
  - It is the value of V_{GS} until which the drain current I_D remains zero.

D-MOSFET Transfer Characteristics

- Fig. 18 shows the transfer characteristics of a N-channel and P-channel D-MOSFETs.

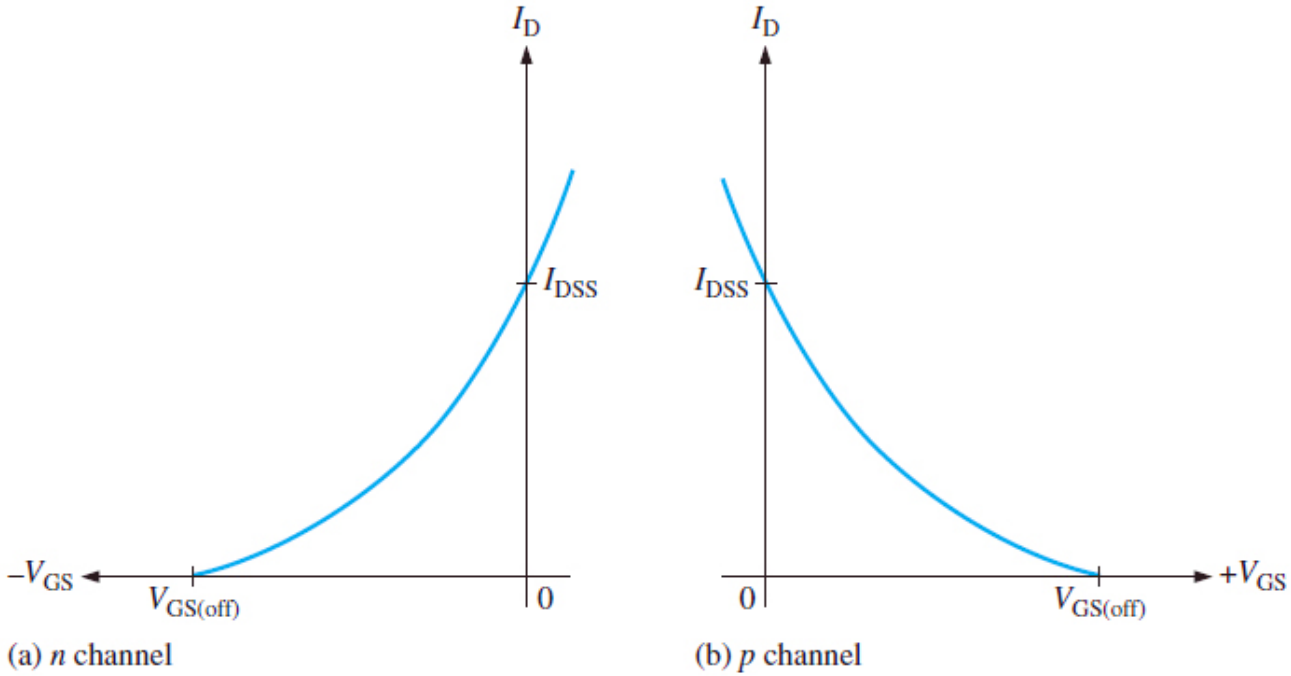


Fig. 18 General transfer characteristics of D-MOSFET

D-MOSFET Transfer Characteristics

- The D-MOSFET can operate with either positive or negative gate voltages.
- The point on the curves where V_{GS}=0 corresponds to I_{DSS}.
- The point where $I_D = 0$ corresponds to cut-off voltage $V_{GS(off)}$.
- The cut-off voltage $V_{GS(off)}$ and pinch-off voltage V_P are equal in magnitude but opposite in sign, i.e., $V_{GS(off)} = -V_P$.

References

- David A. Bell, “*Electronic Devices and Circuits*”, Oxford University Press, 5th Edition, 2016
- Thomas L. Floyd, *"Electronic Devices",* Pearson Education, 9th Edition, 2012