# Field-Effect Transistors

***Topics Covered from Module 2:*** *Introduction, JFET: Construction and Operation, JFET Drain Characteristics and Parameters, JFET Transfer Characteristics, Square law expression for $I_D$, Input resistance, MOSFET: Depletion and Enhancement type MOSFET – Construction, Operation, Characteristics and Symbols, CMOS.*

## Introduction

The Field-Effect Transistor (FET) is a three-terminal device that uses electric field to control the current flowing through the device. It has three terminals – Source (S), Drain (D) and Gate (G).

FETs are unipolar devices because they operate only with one type of charge carrier. The two main types of FETs are the Junction Field-Effect Transistor (JFET) and the Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). The term *field-effect* relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminals (gate).

An FET is a voltage-controlled device, where the voltage between two of the terminals (gate and source) controls the current through the device. A major advantage of FETs is their very high input resistance. Because of their nonlinear characteristics, they are generally not as widely used in amplifiers as BJTs, except where very high input impedances are required. However, FETs are the preferred device in low-voltage switching applications because they are generally faster than BJTs when turned on and off.

## JFET

The JFET (Junction Field-Effect Transistor) is a type of FET that operates with a reverse-biased *pn*-junction to control current in a channel. Depending on their structure, JFETs are classified into N-channel JFET and P-channel JFET.

### N-Channel JFET

### Construction


(a) Basic structure (b) Symbol

Fig. 1 N-channel JFET

Fig. 1 (a) shows the basic shows the basic structure of an N-channel JFET. Wire leads are connected to each end of the N-channel; the drain is at the upper end, and the source is at the

lower end. Two *p*-type regions are diffused in the *n*-type material to form a channel, and both *p*-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the *p*-type regions. The symbol of a N-channel JFET is shown in Fig. 1 (b).

## Operation

To illustrate the operation of a JFET, Fig. 2 shows dc bias voltages applied to an N-channel JFET. $V_{DS}$ provides a drain-to-source voltage and supplies current from drain to source. $V_{GS}$ sets the reverse-bias voltage between the gate and the source, as shown.

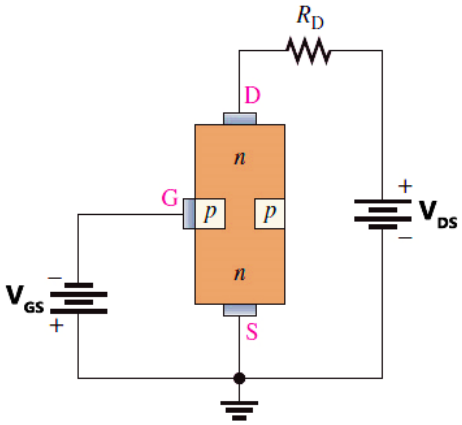



Fig. 2 A biased N-channel JFET

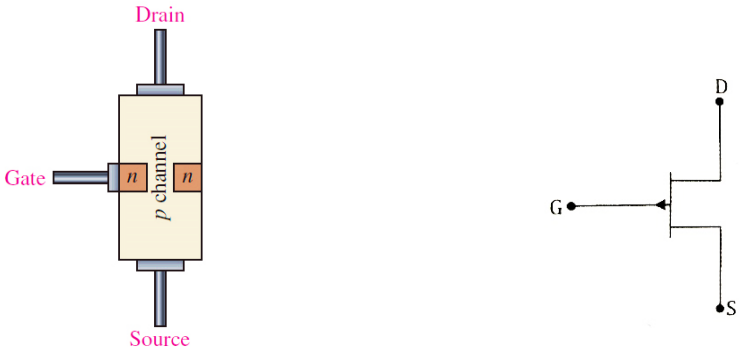
The JFET is always operated with the gate-source *pn*-junction reverse-biased. Reverse-biasing of the gate-source junction with a negative gate voltage produces a depletion region along the *pn*-junction, which extends into the N-channel and thus increases its resistance by restricting the channel width. The channel width and thus, the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, $I_D$.

The depletion region is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.

**Note:** In an N-channel JFET, $V_{GS}$ is negative and $V_{DS}$ is positive.

## P-Channel JFET

## Construction




**(a) Basic structure** **(b) Symbol**

Fig. 3 P-channel JFET

Fig. 3 (a) shows the basic shows the basic structure of a P-channel JFET. Wire leads are connected to each end of the P-channel; the drain is at the upper end, and the source is at the

lower end. Two *n*-type regions are diffused in the *p*-type material to form a channel, and both *n*-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the *n*-type regions. The symbol of a P-channel JFET is shown in Fig. 3 (b).

## Operation

Fig. 4 shows dc bias voltages applied to a P-channel JFET. $V_{DS}$ provides a drain-to-source voltage and supplies current from drain to source. $V_{GS}$ sets the reverse-bias voltage between the gate and the source, as shown.

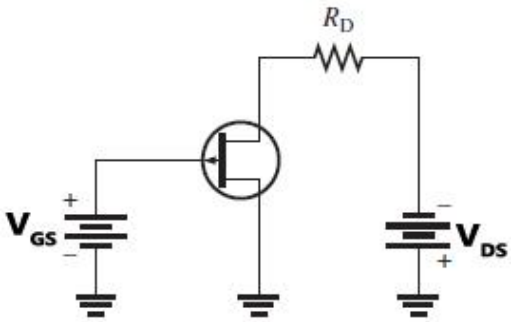



Fig. 4 A biased P-channel JFET

The JFET is always operated with the gate-source *pn*-junction reverse-biased. Reverse-biasing of the gate-source junction with a positive gate voltage produces a depletion region along the *pn*-junction, which extends into the P-channel and thus increases its resistance by restricting the channel width. The channel width and thus, the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, $I_D$.

The depletion region is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.

**Note:** In a P-channel JFET, $V_{GS}$ is positive and $V_{DS}$ is negative.

## JFET Characteristics and Parameters

## Characteristics of N-Channel JFET

## Drain Characteristics

Drain characteristics is the plot of $V_{DS}$ vs $I_D$ for constant values of $V_{GS}$.

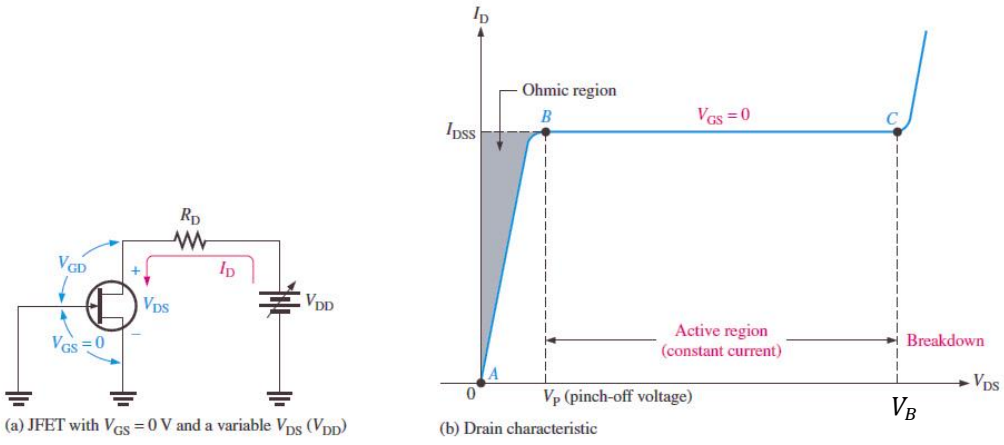



Fig. 5 Drain characteristic of N-channel JFET for $V_{GS} = 0$

Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0\ V$) as shown in Fig. 5 (a). As $V_{DD}$ (and thus $V_{DS}$) is increased from 0 V, $I_D$ will increase proportionally, as shown in the graph of Fig. 5 (b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the *ohmic region* because $V_{DS}$ and $I_D$ are related by Ohm's law.

At point B in Fig. 5 (b), the curve levels off and enters the active region where $I_D$ becomes constant. As $V_{DS}$ increases from point B to point C, the reverse-bias voltage from gate to drain ($V_{GD}$) produces a depletion region large enough to offset the increase in $V_{DS}$, thus keeping $I_D$ relatively constant.

**Pinch-off Voltage ($V_P$):** It is the value of $V_{DS}$ at which $I_D$ becomes constant for $V_{GS} = 0\ V$ (point B on the curve in Fig. 5 (b)). For a given JFET, $V_P$ has a fixed value. A continued increase in $V_{DS}$ above the pinch-off voltage produces an almost constant drain current. This value of drain current is **$I_{DSS}$ (Drain to Source current with gate Shorted)**.

**$I_{DSS}$** is the maximum drain current that a specific JFET can produce when the gate is shorted, i.e., $V_{GS} = 0\ V$.

**Breakdown:** When $V_{DS}$ exceeds the breakdown voltage $V_B$ (point C in Fig. 5 (b)), breakdown occurs and $I_D$ begins to increase very rapidly with any further increase in $V_{DS}$. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points B and C on the graph).

Fig. 6 shows drain characteristics of N-channel for different values of $V_{GS}$.

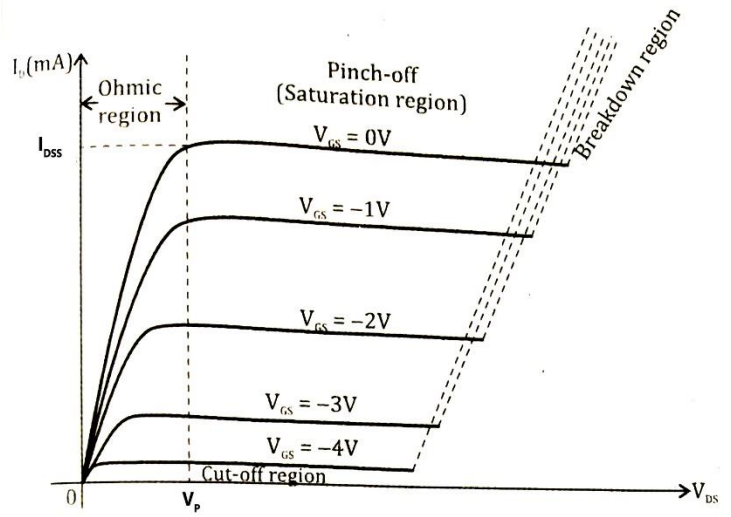



Fig. 6 Drain characteristic of N-channel JFET

The different regions on the JFET drain characteristics are summarized as below:

i) **Ohmic Region:** In this region, the channel of JFET obeys Ohm's law.

ii) **Pinch-off Region/Saturation Region:** In this region, $I_D$ is maximum and remains constant for a given $V_{GS}$.

iii) **Breakdown Region:** In this region, the *pn*-junction breaks down and $I_D$ increases abruptly. The JFET loses its ability to control $I_D$.

iv) **Cut-off Region:** In this region, JFET if OFF, i.e., $I_D = 0$.

## Transfer Characteristics

Transfer characteristics is the plot of $V_{GS}$ vs $I_D$ for constant values of $V_{DS}$. Fig. 7 shows the transfer characteristic curve for an N-channel JFET. This curve is also known as a transconductance curve.

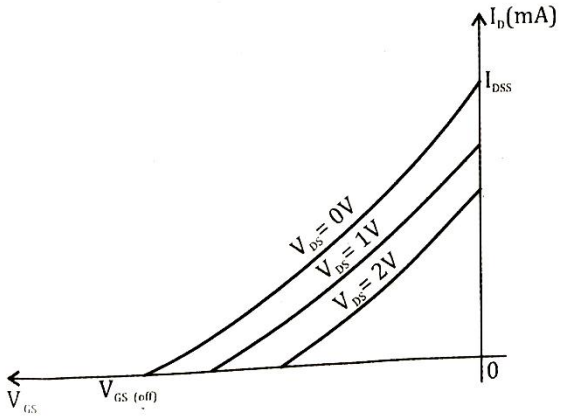



Fig. 7 Transfer characteristic of N-channel JFET

As observed, a range of $V_{GS}$ values from 0 to $V_{GS(off)}$ controls the amount of drain current. $V_{GS(off)}$ is called the *cut-off voltage*.

**Cut-off Voltage ($V_{GS(off)}$):** It is the value of $V_{GS}$ that makes $I_D$ approximately zero. The cut-off voltage $V_{GS(off)}$ and pinch-off voltage $V_P$ are always equal in magnitude but opposite in sign, i.e., $V_{GS(off)} = -V_P$. $V_{GS(off)}$ is negative for an N-channel JFET and positive for a P-channel JFET.

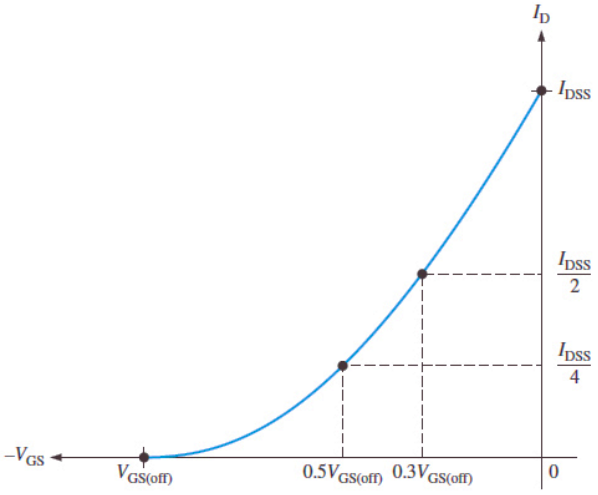



Fig. 8 N-channel JFET universal transfer characteristic curve

Fig. 8 is a general (universal) transfer characteristic curve that illustrates graphically the relationship between $V_{GS}$ and $I_D$. This curve shows that,

$I_D = 0$ when $V_{GS} = V_{GS(off)}$

$I_D = \frac{I_{DSS}}{4}$ when $V_{GS} = 0.5\ V_{GS(off)}$

$I_D = \frac{I_{DSS}}{2}$ when $V_{GS} = 0.3\ V_{GS(off)}$

and $I_D = I_{DSS}$ when $V_{GS} = 0$

## Square Law Expression for $I_D$

The transfer characteristics of a JFET can be expressed as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

This is called the *square law expression for* $I_D$.

In terms of pinch-off voltage, the equation can be written as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

This is known as *Shockley's equation*.

## JFET Forward Transconductance

The forward transconductance (transfer conductance), $g_m$, is the change in drain current ($\Delta I_D$)for a given change in gate-to-source voltage ($\Delta V_{GS}$) with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

## Input Resistance

As JFET operates with its gate-source junction reverse-biased, its input resistance at the gate is very high. This high input resistance is one advantage of the JFET over the BJT. The input resistance is given as

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

Here $I_{GSS}$ is the gate reverse current at a certain gate-to-source voltage $V_{GS}$.

**Note:** In an N-channel JFET, $V_{GS}$ is negative and $V_{DS}$ is positive. $V_{GS(off)}$ is negative.

## Characteristics of P-Channel JFET

## Drain Characteristics

Drain characteristics is the plot of $V_{DS}$ vs $I_D$ for constant values of $V_{GS}$. Fig. 9 shows the drain characteristics of a P-channel JFET.

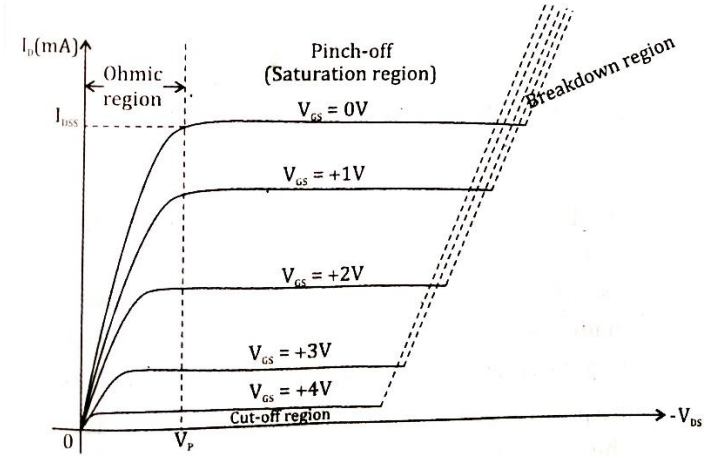



Fig. 9 Drain characteristics of P-channel JFET

## Transfer Characteristics

Transfer characteristics is the plot of $V_{GS}$ vs $I_D$ for constant values of $V_{DS}$. Fig. 10 shows the transfer characteristics of a P-channel JFET.

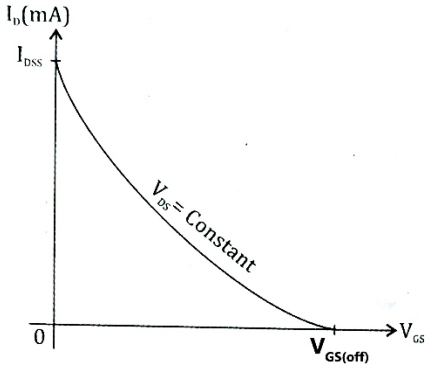



Fig. 10 Transfer characteristics of P-channel JFET

**Note:** In a P-channel JFET, $V_{GS}$ is positive and $V_{DS}$ is negative. $V_{GS(off)}$ is positive.

# MOSFET

The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) is a type of FET which has no *pn*-junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide ($SiO_2$) layer. The two basic types of MOSFETs are Enhancement type (E-MOSFET) and Depletion type (D-MOSFET). Of the two types, the Enhancement MOSFET is more widely used. Because polycrystalline silicon is now used for the gate material instead of metal, MOSFETs are sometimes called IGFETs (Insulated-Gate FETs).

The MOSFET has two modes of operation – enhancement mode and depletion mode. An E-MOSFET can be operated only in enhancement mode and has no depletion mode. A D-MOSFET can be operated in either depletion mode or enhancement mode and hence it is also called depletion/enhancement MOSFET.

## Enhancement Type MOSFET (E-MOSFET)

## Construction

An E-MOSFET can be operated only in enhancement mode and has no depletion mode. An E-MOSFET has no structural channel. The basic structure of an N-channel E-MOSFET is shown in Fig. 11 (a).

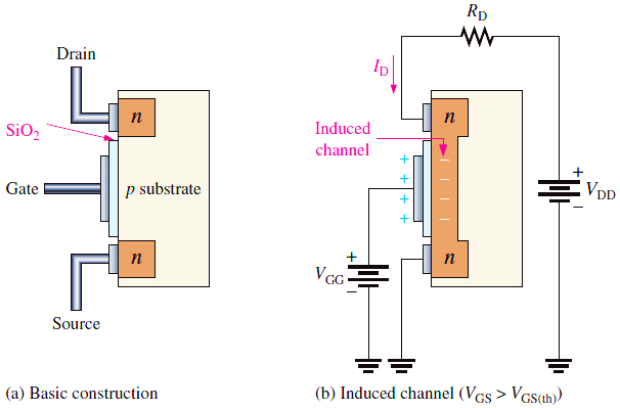



Fig. 11 Construction and operation of N-channel E-MOSFET

A *p*-type substrate is the basic structure upon which *n*-type regions are created by diffusion. An oxide ($SiO_2$) layer which acts as an insulator covers the entire *p*-type substrate and *n*-type regions. By etching proper openings through the oxide layer, metal contacts for source and drain connections are made to the *n*-regions. The gate contact is formed on the surface of the oxide layer. The gate is electrically insulated from both *n*-type regions and the *p*-type substrate.

Regardless of the polarity of applied voltage, no electrons can flow from source to drain because the *n*-type source, *p*-type substrate and *n*-type drain behave as two *pn*-junctions connected back-to-back and one of the *pn*-junctions is always reverse biased.

## Operation

Consider a positive voltage is applied between gate and source as shown in Fig. 11 (b). As the oxide layer is an insulator sandwiched between two conductive regions, a capacitive effect is formed. The metal surface which is gate and the conducting substrate act as the capacitor plates.

When a positive charge is applied to one plate of the capacitor, a corresponding negative charge is induced on the opposite plate due to the electric field between the plates. In this case, the positive potential at the gate induces negative charges in the *p*-type substrate. This charge results from minority carriers (electrons) attracted towards the area of the gate. As the number of electrons reaching the region increases, the N-channel is formed gradually and resistance between source and drain decreases. The greater the gate potential, the lower the channel resistance and higher the drain current $I_D$. This process is called *enhancement* and the resulting device is called *enhancement type* MOSFET (E-MOSFET).

Fig. 12 shows the symbols of N-channel and P-channel E-MOSFET.


(a) N-channel E-MOSFET (b) P-channel E-MOSFET

Fig. 12 Symbols of E-MOSFET

In a P-channel E-MOSFET, the substrate is of *n*-type and the diffused regions are of *p*-type. When a negative voltage is applied between the gate and source, a P-channel is induced in the *n*-type substrate. The operation of P-channel E-MOSFET can be explained on the same grounds as of N-channel, except the voltage polarities are opposite to those of the N-channel.

## Depletion Type MOSFET (D-MOSFET)

## Construction

A D-MOSFET can be operated in either depletion mode or enhancement mode and hence it is also called depletion/enhancement MOSFET. Fig. 13 shows the basic structure of N-channel and P-channel D-MOSFETs.

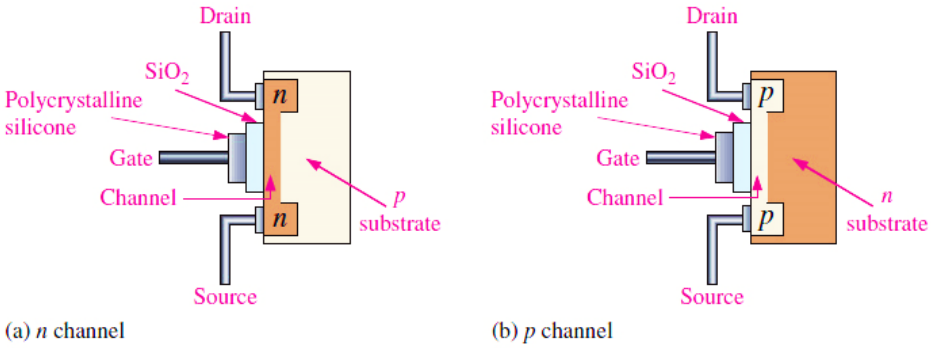



Fig. 13 Basic structure of D-MOSFETs

The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. In an N-channel D-MOSFET, the substrate is of *p*-type and the diffused regions are of *n*-type and the channel is formed by doping *n*-type material adjacent to the gate. In a P-channel D-MOSFET, the substrate is of *n*-type and the diffused regions are of *p*-type and the channel is formed by doping *p*-type material adjacent to the gate.

## Operation

Consider a N-channel D-MOSFET. Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied. The N-channel D-MOSFET operates in the depletion mode when a negative gate-to-source voltage is applied and in the enhancement mode when a positive gate-to-source voltage is applied. D-MOSFETs are generally operated in the depletion mode.

## Depletion Mode

When a negative voltage is applied between the gate and source, the negative charges on the gate induce an equal amount of positive charges (holes) on the other side of the oxide layer. This results in the recombination of holes with electrons in the channel and reduces the number of free electrons available. This makes the channel depleted of charge carriers which increases the effective resistance of the channel. As the $V_{GS}$ is made more and more negative, the channel resistance becomes more and more, resulting in lesser drain current. At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero.

## Enhancement Mode

When a positive voltage is applied between the gate and source, free electrons are induced in the N-channel, which enhances the channel conductivity and thus $I_D$ increases.

Fig. 14 shows the symbols of N-channel and P-channel D-MOSFET.


Fig. 14 Symbols of D-MOSFET

The operation of P-channel D-MOSFET can be explained on the same grounds as of N-channel, except the voltage polarities are opposite to those of the N-channel.

## MOSFET Characteristics and Parameters

## Drain Characteristics

## E-MOSFET Drain Characteristics

Drain characteristics is the plot of $V_{DS}$ vs $I_D$ for constant values of $V_{GS}$. Fig. 15 shows the drain characteristics of an N-channel E-MOSFET.

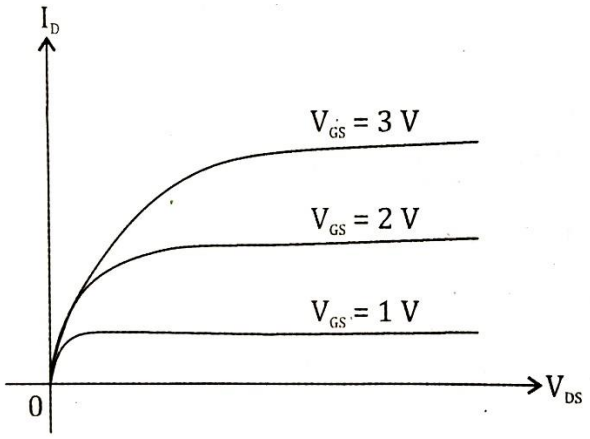



Fig. 15 Drain characteristics of N-channel E-MOSFET

## D-MOSFET Drain Characteristics

Drain characteristics is the plot of $V_{DS}$ vs $I_D$ for constant values of $V_{GS}$. Fig. 16 shows the drain characteristics of an N-channel D-MOSFET. The N-channel D-MOSFET is in depletion mode when $V_{GS}$ is negative and in enhancement mode when $V_{GS}$ is positive.

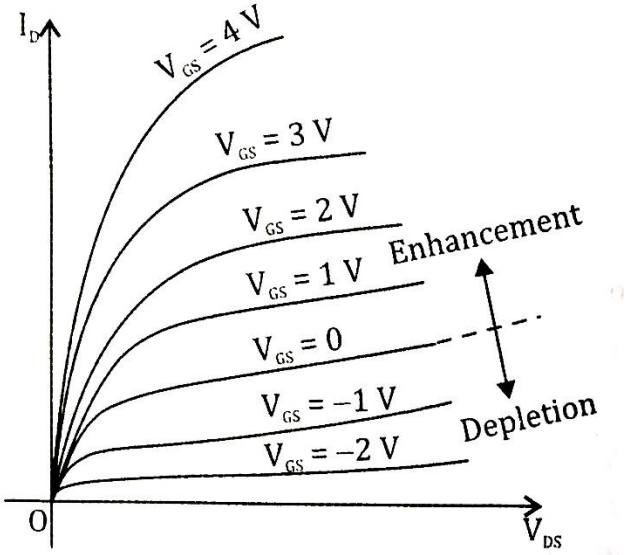



Fig. 16 Drain characteristics of N-channel D-MOSFET

The drain characteristics of P-channel E-MOSFET is similar to that N-channel, but in P-channel, $V_{DS}$ and $V_{GS}$ are negative. The P-channel D-MOSFET is in depletion mode when $V_{GS}$ is positive and in enhancement mode when $V_{GS}$ is negative.

# Transfer Characteristics

## E-MOSFET Transfer Characteristics

Transfer characteristics is the plot of $V_{GS}$ vs $I_D$ for constant values of $V_{DS}$. Fig. 17 shows the transfer characteristics of N-channel and P-channel E-MOSFETs.

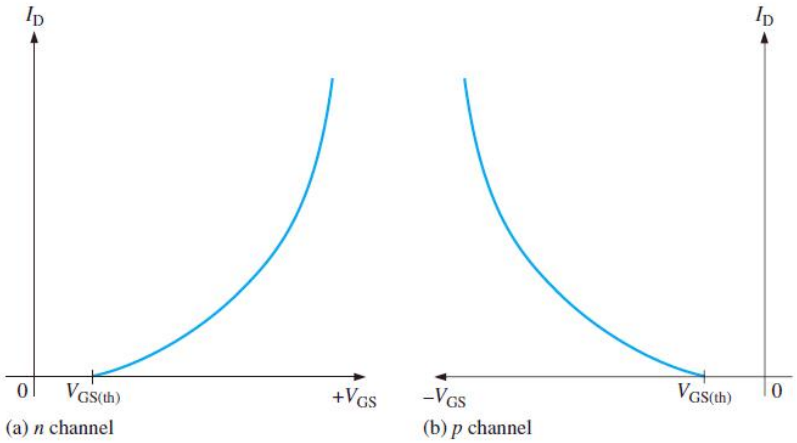



Fig. 17 General transfer characteristics of E-MOSFET

The E-MOSFET uses only channel enhancement. Therefore, an N-channel device requires a positive $V_{GS}$, and a P-channel device requires a negative $V_{GS}$. From the characteristic, there is no drain current when $V_{GS} = 0$. Therefore, the E-MOSFET does not have a significant $I_{DSS}$ parameter. Also, there is ideally no drain current until $V_{GS}$ reaches a certain nonzero value called the threshold voltage, $V_{GS(th)}$.

**Threshold voltage $V_{GS(th)}$:** It is the value of $V_{GS}$ until which the drain current $I_D$ remains zero.

The equation for the E-MOSFET transfer characteristic curve is given by

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2$$

The constant $K$ depends on the particular MOSFET and can be determined from the datasheet by taking the specified value of $I_D$, called $I_{D(on)}$, at the given value of $V_{GS}$.

## D-MOSFET Transfer Characteristics

Transfer characteristics is the plot of $V_{GS}$ vs $I_D$ for constant values of $V_{DS}$. Fig. 18 shows the transfer characteristics of a N-channel and P-channel D-MOSFETs.

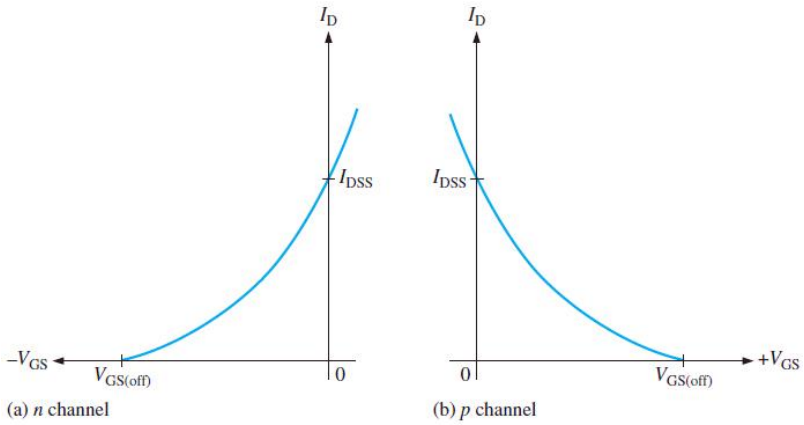



Fig. 18 General transfer characteristics of D-MOSFET

The D-MOSFET can operate with either positive or negative gate voltages. The point on the curves where $V_{GS}$=0 corresponds to $I_{DSS}$. The point where $I_D = 0$ corresponds to cut-off voltage $V_{GS(off)}$.

The cut-off voltage $V_{GS(off)}$ and pinch-off voltage $V_P$ are equal in magnitude but opposite in sign, i.e., $V_{GS(off)} = -V_P$.

The drain current $I_D$ is given by the square law expression as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

# CMOS

CMOS is the complementary metal oxide semiconductor, wherein two enhancement type MOSFETs – one N-type (NMOS) and one P-type (PMOS), are connected as a complementary pair. The two gates are connected to form the input terminal and the two drains are connected to form the output terminal as shown in Fig. 19 (a).

## CMOS Inverter

CMOS is used in digital circuits and one basic application of CMOS is as an inverter as shown in Fig. 19 (a). An inverter is a logic circuit that inverts the applied signal, i.e., if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an applied input level of 0 V will result in an output level of 5 V and vice versa.

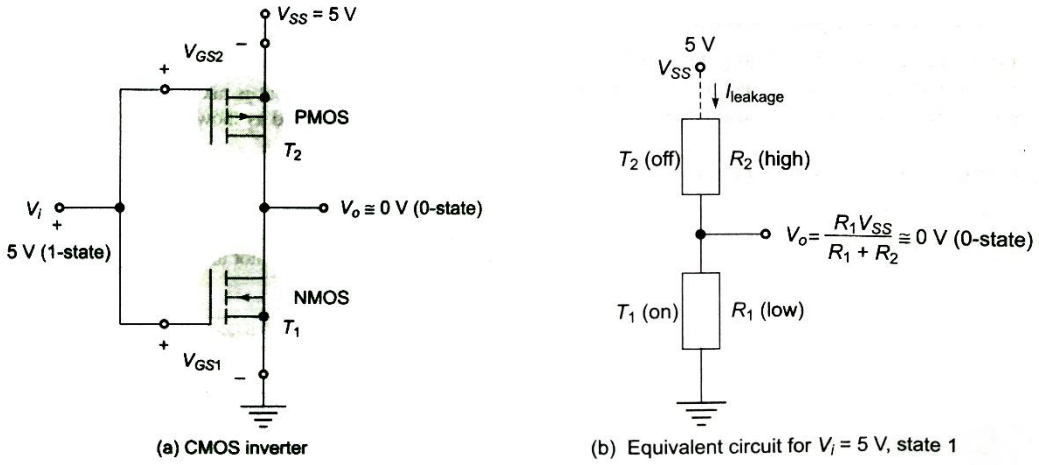



Fig. 19 CMOS inverter

The source terminal of PMOS ($T_2$) is connected to $V_{SS} = 5\ V$, while the source terminal of NMOS ($T_1$) is grounded. The two gates are connected to form the input terminal and the two drains are connected to form the output terminal.

## Operation

**i) When the input $V_i = 5\ V$ (1-state)**

$$V_{GS_2} = V_i - V_{SS} = 5 - 5 = 0\ V$$

So, $T_2$ is nonconducting (OFF) and offers high resistance $R_2$ and draws only leakage current.

$$V_{GS_1} = V_i = 5\ V > V_T$$

So, $T_1$ is conducting (ON) and offers very low resistance $R_1$.

The equivalent circuit in this state is as shown in Fig. 19 (b). From the circuit,

$$V_o = \frac{R_1}{R_1 + R_2} V_{SS} \approx 0\ V$$

Hence output $\boldsymbol{V_o = 0\ V}$ **(0-state).**

**ii) When the input $\boldsymbol{V_i = 0\ V}$ (0-state)**

$$V_{GS_2} = V_i - V_{SS} = 0 - 5 = -5\ V$$

So, $T_2$ is conducting (ON) and offers very low resistance $R_2$.

$$V_{GS_1} = V_i = 0\ V$$

So, $T_1$ is nonconducting (OFF) and offers high resistance $R_1$.

From the circuit,

$$V_o = \frac{R_1}{R_1 + R_2} V_{SS} \approx V_{SS} = 5\ V$$

Hence output $\boldsymbol{V_o = 5\ V}$ **(1-state).**

Thus, 1-state input produces 0-state output and 0-state input produces 1-state output. That is, the circuit acts as an inverter.

It is observed that, in any of the output states, only one transistor is turned on. As the transistors are series connected, no current is drawn from the battery source in either of the two states. Current is drawn from the battery only during state transitions. Hence, CMOS circuits draw extremely low power from the battery and so their energy consumption is very small. This makes CMOS a popular choice for digital applications.

## Advantages of CMOS

- The drain current is very low and flows mainly during transition from one state to the other (ON/OFF)
- The power drawn in steady state is extremely low and energy consumption is very small
- High input impedance
- Fast switching speeds

# Numerical Examples

1. A particular p-channel JFET has a $V_{GS(off)} = +4\ V$. What is $I_D$ when $V_{GS} = +6\ V$? What is the value of $V_P$?

   *Solution:*

   The p-channel JFET requires a positive gate-to-source voltage.

   The more positive the voltage, the less the drain current.

   When $V_{GS} = 4\text{V}$, $I_D = 0$.

Any further increase in $V_{GS}$ keeps the JFET cut off, so $I_D$ remains 0.

So when $V_{GS} = +6\,V$, $I_D = 0$.

$V_P = -V_{GS(off)} = -4\,V$

2. For a JFET, $I_{DSS}$ of 9 mA for $V_{GS(off)} = -8$ V (max). Determine drain current for $V_{GS} = 0\,V, -1\,V, -4$ V.

*Solution:*

Given $I_{DSS} = 9mA$, $V_{GS(off)} = -8V$

i) For $V_{GS} = 0V$,

$$I_D = I_{DSS} = 9mA$$

ii) For $V_{GS} = -1V$,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 9\times10^{-3}\left[1 - \frac{-1}{-8}\right]^2$$

$$= 6.89\,mA$$

iii) For $V_{GS} = -4V$,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 9\times10^{-3}\left[1 - \frac{-4}{-8}\right]^2$$

$$= 2.25\,mA$$

3. For an N-channel JFET, if $I_{DSS} = 8$ mA and $V_P = -5$ V, calculate $I_D$ at $V_{GS} = -3$ V and $V_{GS}$ at $I_D = 3$ mA.

   *Solution:*

Given

$$I_{DSS} = 8\ mA$$

$$V_P = V_{GS(OFF)} = -5\ V$$

WKT

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

At $V_{GS} = -3V$,

$$I_D = 8 \times 10^{-3}\left(1 - \frac{-3}{-5}\right)^2$$

$$= 1.28\ mA$$

WKT

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$\therefore \left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2 = \frac{I_D}{I_{DSS}}$$

$$1 - \frac{V_{GS}}{V_{GS(OFF)}} = \pm\sqrt{\frac{I_D}{I_{DSS}}}$$

$$\frac{V_{GS}}{V_{GS(OFF)}} = 1 \mp \sqrt{\frac{I_D}{I_{DSS}}}$$

$$V_{GS} = V_{GS(OFF)}\left[1 \mp \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

If $I_D = 3\text{ mA}$,

$$V_{GS} = -5\left[1 \mp \sqrt{\frac{3}{8}}\right]$$

$$= -1.94\text{ V} \quad \text{or} \quad -8.06\text{ V}$$

As $V_P = -5\text{ V}$, $I_D$ will be 0 if $V_{GS} > V_P$.

$\therefore$ $V_{GS}$ cannot be $-8.06\text{ V}$ given $I_D = 3\text{ mA}$.

$\therefore$ $V_{GS} = \underline{\underline{-1.94\text{ V}}}$

4. For an N-channel JFET, if $I_{DSS} = 9\text{ mA}$ and $V_P = -6\text{ V}$, calculate $I_D$ at $V_{GS} = -4\text{ V}$ and $V_{GS}$ at $I_D = 3\text{ mA}$.

   *Solution:*

Given

$$I_{DSS} = 9\text{ mA}$$

$$V_P = V_{GS(OFF)} = -6\text{ V}$$

WKT $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

At $V_{GS} = -4\text{ V}$,

$$I_D = I_{DSS}\left(1 - \frac{-4}{-6}\right)^2$$

$$= 9\times10^{-3}\left(1 - \frac{2}{3}\right)^2$$

$$= \underline{\underline{1\text{ mA}}}$$

WKT

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$\therefore \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = \frac{I_D}{I_{DSS}}$$

$$1 - \frac{V_{GS}}{V_{GS(off)}} = \pm\sqrt{\frac{I_D}{I_{DSS}}}$$

$$\frac{V_{GS}}{V_{GS(off)}} = 1 \mp \sqrt{\frac{I_D}{I_{DSS}}}$$

$$V_{GS} = V_{GS(off)}\left[1 \mp \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

At $I_D = 3\,mA$,

$$V_{GS} = -6\left(1 \mp \sqrt{\frac{3}{9}}\right)$$

$$= -6\left(1 \mp \sqrt{0.33}\right)$$

$$= -2.535\,V \text{ or } -9.46\,V$$

As $V_p = -6V$, $I_D$ will be 0 if $V_{GS} > V_p$

$\therefore V_{GS}$ cannot be $-9.46V$, given $I_D = 3\,mA$

$\therefore V_{GS} = -2.535V$

5. A certain JFET has $I_{GSS}$ of $-2\,nA$ for $V_{GS} = -20\,V$. Determine the input resistance.

   *Solution:*

Given

$$V_{GS} = -20V$$

$$I_{GSS} = -2\,nA = -2 \times 10^{-9}$$

$$R_{IN} = \left| \frac{V_{GS}}{I_{GS}} \right|$$

$$= \left| \frac{-20}{-2 \times 10^{-9}} \right|$$

$$= 10 \times 10^{9}\ \Omega$$

$$= 10000\ M\Omega$$

6. For an E-MOSFET, $I_{D(ON)} = 500\ mA$ (minimum) at $V_{GS} = 10\ V$ and $V_{GS(th)} = 1\ V$. Determine the drain current for $V_{GS} = 5\ V$.

   *Solution:*

Given $I_{D(on)} = 500\ mA$,

$V_{GS} = 10\ V$

$V_{GS(th)} = 1\ V$

WKT, $I_D = K (V_{GS} - V_{GS(th)})^2$

$$K = \frac{I_D}{(V_{GS} - V_{GS(th)})^2}$$

$$= \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500 \times 10^{-3}\ A}{[(10-1)V]^2} = 6.17\ mA/V^2$$

Now, If $V_{GS} = 5V$.

$$I_D = K\left(V_{GS} - V_{GS(Th)}\right)^2$$

$$= 6.17\,mA/V^2\left[(5-1)V\right]^2$$

$$= 6.17 \times 4^2\ mA$$

$$= 98.7\,mA$$

7. For E-MOSFET, determine the value of $I_D$, if $I_{D(ON)} = 4\ mA, V_{GS(ON)} = 6\ V, V_T = 4\ V$ and $V_{GS} = 8\ V$.

*Solution:*

Given $I_{D(ON)} = 4\,mA$

$V_{GS(ON)} = 6V$

$V_T = V_{GS(Th)} = 4V$

$V_{GS} = 8V$.

WKT, $I_D = K\left(V_{GS} - V_{GS(Th)}\right)^2$

$$\therefore K = \frac{I_{D(ON)}}{\left(V_{GS(ON)} - V_{GS(Th)}\right)^2}$$

$$= \frac{4\times10^{-3}}{(6-4)^2} = 1\times10^{-3}$$

Now,

$$I_D = K(V_{GS} - V_{GS(th)})^2$$
$$= 1\times10^{-3}(8-4)^2$$
$$= 16\ mA$$

8. For a certain D-MOSFET, $I_{DSS} = 10\ mA$ and $V_{GS(off)} = -8\ V$.

   (a) Is this an n-channel or a p-channel device?

   (b) Calculate $I_D$ at $V_{GS} = -3\ V$.

   (c) Calculate $I_D$ at $V_{GS} = +3\ V$.

   *Solution:*

a) The $V_{GS(off)}$ is negative.

∴ this is an n-channel D-MOSFET

b) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$
$$= 10\times10^{-3}\left(1 - \frac{-3}{-8}\right)^2$$
$$= 3.91\ mA$$

c) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$
$$= 10\times10^{-3}\left(1 - \frac{+3}{-8}\right)^2$$
$$= 18.9\ mA$$

9. For a certain D-MOSFET, $I_{DSS} = 18\ mA$ and $V_{GS(off)} = +10\ V$.

   (a) Is this an n-channel or a p-channel device?

   (b) Calculate $I_D$ at $V_{GS} = +4\ V$.

   (c) Calculate $I_D$ at $V_{GS} = -4\ V$.

   *Solution:*

a) The $V_{GS(OFF)}$ is positive.

$\therefore$ This is a p-channel D-MOSFET

b) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$= 18\times10^{-3}\left(1 - \frac{+4}{+10}\right)^2$$

$$= 6.48\ mA$$

c) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-4}{+10}\right)^2$$

$$= 18\times10^{-3}(1 + 0.4)^2$$

$$= 35.28\ mA$$

# Questions

1. Explain the construction and operation of JFET with necessary diagram. ***(MQP '18 – 7M)***
2. Explain the basic structure and operation of JFET with neat diagrams. ***(Jan '19 – 8M)***
3. Explain the construction, working and characteristics of N-channel JFET. ***(Jan '20 – 9M, Jul '19 – 9M)***
4. Explain construction and operation of N-channel JFET. Draw transfer and drain characteristics. ***(Sep '20 – 8M)***
5. Explain the construction and operation of a P-channel JFET. ***(MQP '18 – 8M)***
6. Explain the drain and transfer characteristics of JFET with neat circuit diagram. ***(Jan '19 – 8M)***
7. Explain the characteristics of N-channel JFET. ***(MQP '18 – 8M)***
8. Explain the characteristics of P-channel JFET.
9. With neat diagrams, explain the characteristics of JFET and write the equation of square law.
10. Explain the construction, working and characteristics of enhancement type MOSFET. ***(Jan '20 – 9M, Jul '19 – 9M)***
11. Explain the construction and working of N-channel enhancement type MOSFET.
12. Explain the construction and working of P-channel enhancement type MOSFET. ***(MQP '18 – 8M)***
13. Explain the operation of an enhancement MOSFET with neat circuit diagram. ***(Jan '19 – 6M)***
14. Explain construction and operation of N-channel depletion MOSFET. ***(Sep '20 – 8M)***
15. Explain construction and operation of P-channel depletion MOSFET.
16. What is MOSFET? Explain D-MOSFET and E-MOSFET transfer characteristics. ***(MQP '18 – 8M)***
17. With neat diagram, explain the characteristics of an enhancement type MOSFET. ***(MQP '18 – 8M)***
18. With neat diagrams, explain the characteristics of MOSFET.
19. Explain CMOS as an inverter with neat circuit diagram. Give its equivalent circuit and its advantages. ***(Jan '19 – 8M)***
20. With a neat circuit diagram, explain the operation of a CMOS inverter. ***(Sep '20 – 6M, Jan '20 – 6M, Jul '19 – 6M, MQP '18 – 7M)***
21. An N-channel JFET has $I_{DSS} = 8$ mA and $V_P = -4$ V, calculate $I_D$ at $V_{GS} = -1$ V and $V_{GS} = -2$ V. ***(Sep '20 – 6M)***
22. For an N-channel JFET, if $I_{DSS} = 9$ mA and $V_P = -6$ V, calculate $I_D$ at $V_{GS} = -4$ V and $V_{GS}$ at $I_D = 3$ mA. ***(Jan '20 – 5M)***

23. For an N-channel JFET, if $I_{DSS} = 8$ mA and $V_P = -5$ V, calculate $I_D$ at $V_{GS} = -3$ V and $V_{GS}$ at $I_D = 3$ mA. ***(Jul '19 – 5M)***
24. For a JFET, $I_{DSS}$ of 9 mA for $V_{GS(off)} = -8$ V (max). Determine drain current for $V_{GS} = -4$ V. ***(Jan '19 – 4M)***
25. A certain JFET has $I_{GSS}$ of $-2$ nA for $V_{GS} = -20$ V. Determine the input resistance. ***(MQP '18 – 4M)***
26. For E-MOSFET, determine the value of $I_D$, if $I_{D(ON)} = 4$ mA, $V_{GS(ON)} = 6$ V, $V_T = 4$ V and $V_{GS} = 8$ V. ***(Jan '20 – 5M, MQP '18 – 4M)***

# References

1. Thomas L. Floyd, ***"Electronic Devices"***, Pearson Education, Ninth Edition, 2012.
2. D.P. Kothari, I. J. Nagrath, ***"Basic Electronics"***, McGraw Hill Education (India) Private Limited, Second Edition, 2014.