# Question Bank for Basic Electronics (17ELN15/25)

Module – 1
Semiconductor Diodes and Applications

1. Explain the operation of pn junction diode under forward and reverse bias conditions with the help of V-I characteristics curve.   *(Dec '17 – 6M, Dec '16 – 6M, Jun '16 – 6M)*

2. Explain briefly the pn junction diode characteristics.   *(Jun '17 – 6M)*

3. Draw and explain the V-I characteristics of a Si (Silicon) diode.
      (Dec '15 – 8M, Dec '14 – 5M)

4. Draw and explain the V-I characteristics of a Ge (Germanium) diode.   *(Jun '15 – 5M)*

5. Define following diode parameters: (i) Static resistance (ii) Dynamic resistance (iii) Knee voltage (iv) Forward voltage drop (v) Maximum forward current (vi) Reverse saturation current (vii) Reverse breakdown voltage (viii) Peak inverse voltage (PIV) (ix) Maximum power rating   *(Dec '16 – 5M, MQP '15 – 6M)*

6. Explain the different diode approximation with neat figures.

7. With appropriate circuit diagram, explain the DC load line analysis of semiconductor diode. Also mention the importance of bias point.   *(Dec' 17 – 5M, MQP '14 – 5M)*

8. What is a rectifier?   *(Dec '15)*

9. With a neat circuit diagram, explain the working of a half wave rectifier along with relevant waveforms.   *(Jun '17 – 6M, Jun '15 – 7M, Dec '14 – 7M, MQP '15 – 6M)*

10. Derive the expressions for I_{dc}, V_{dc}, I_{rms}, $V_{rms,}$ regulation, efficiency η_r, ripple factor γ and PIV of a half-wave rectifier.

11. Show that the maximum efficiency of a half wave rectifier is 40.6%.

12. Show that the ripple factor of a half wave rectifier is 1.21.   *(Dec '14)*

13. With a neat circuit diagram, explain the working of a two diode (centre-tapped) full wave rectifier along with relevant waveforms.
      (Dec '17, Jun '17 – 8M, Jun '16 – 6M, Dec '15 – 8M, Jun '15 – 10M, MQP '14 – 8M)

14. With a neat circuit diagram and waveforms, explain the working of centre-tapped full wave rectifier and derive the efficiency for the same.   *(Dec '17 – 10M)*

15. Derive the expressions for I_{dc}, V_{dc}, I_{rms}, $V_{rms,}$ regulation, efficiency η_r, ripple factor γ and PIV of a full-wave rectifier.   *(Dec '17, Jun '15)*

16. Show that the maximum efficiency of a full wave rectifier is 81.2%.   *(Dec '17)*

17. What is ripple factor? Show that the ripple factor of a full wave rectifier is 0.48.
      (Jun '16 – 5M, MQP '14)

18. With a neat circuit diagram, explain the working of a bridge rectifier along with relevant waveforms.   *(Dec '16 – 7M, Dec '15 – 6M)*

19. Derive the expressions for I_{dc}, V_{dc}, I_{rms}, V_{rms}, regulation, efficiency η_r, ripple factor γ and PIV of a bridge rectifier.

20. What is the need for a capacitive filter? Explain.   *(Dec '15)*

21. Briefly explain capacitive filter circuit.   *(Jun '17 – 4M)*

22. With a neat diagram and waveforms, explain the half-wave rectifier with a capacitive filter and derive the expression for ripple factor.   *(Dec '15 – 7M)*

23. With a neat diagram and waveforms, explain the full-wave rectifier with a capacitive filter and derive the expression for ripple factor.

24. Name the junction breakdowns in diodes. Explain them briefly.   *(Jun '16 – 5M)*

25. Distinguish between Zener and Avalanche breakdown.   *(Jun '15 – 6M)*

26. Write a note on voltage regulator circuit.   *(Dec '16 – 5M)*

27. With neat circuit diagrams, explain Zener diode voltage regulator circuit with no load and with load.   *(Dec '17 – 5M, Jun '17 – 6M)*

28. With a neat diagram, explain how Zener diodes can be used for voltage regulation (with no load and with load).   *(Dec '17 – 5M, Jun '16 – 5M, MQP '15 – 6M)*

29. Explain the performance of Zener diode voltage regulator in terms of source and load effects.   *(Dec '14 – 6M)*

30. Discuss the load and line regulation using Zener diode with neat circuit diagram and appropriate expressions.   *(Dec '15 – 6M)*

31. For the circuit shown in the figure, draw the DC load line and locate Q-point.   *(Dec '15 – 4M)*
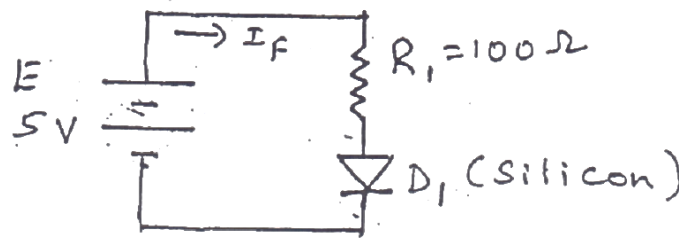
32. Find the value of the series resistance R required to drive a forward current of 1.25 mA through a Germanium diode from a 4.5 V battery. Write the circuit diagram showing all the values.   *(Jun '15 – 4M)*

33. In a half wave rectifier, the input is from 30 V transformer. The load and diode forward resistances are 100 Ω and 10 Ω respectively. Calculate the I_{dc}, I_{rms}, P_{dc}, P_i, η, PIV and regulation factor.   *(Jun '17 – 8M)*

34. A half wave rectifier from a supply 230 V, 50 Hz with a step-down transformer ratio 3:1 to a resistive load of 10 kΩ. The diode forward resistance is 75 Ω and transformer secondary is 10 Ω. Calculate the DC current, DC voltage, efficiency and ripple factor.   *(Dec '17 – 6M)*

35. A transformer with 10:1 turns ratio is connected to a half wave rectifier with supply voltage of 220 sin 210t. If load and forward resistances are 500 Ω and 10 Ω respectively, calculate

the average output voltage, dc output power, ac input power, rectification efficiency and peak inverse voltage. *(Dec '17 – 5M)*

36. The input to a half wave rectifier is given through a 10:1 transformer from a supply given by $230 \sin 314t$ V. If $R_f = 50\,\Omega$ and $R_L = 500\,\Omega$, determine DC load voltage, RMS load voltage, rectification efficiency, DC power delivered to the load. *(Dec '16 – 8M)*

37. A full wave rectifier has a load of 1 kΩ. The ac voltage applied to the diode is $200 - 0 - 200$ V. If diode resistance is neglected, calculate (i) average dc current (ii) average dc voltage. *(Dec '15 – 4M)*

38. A single phase full wave rectifier supplies power to a 1 kΩ load. The AC voltage applied to the diode is $300 - 0 - 300$ V. If diode resistance is 25Ω and that of the transformer secondary negligible, determine load current, average load voltage and rectification efficiency. *(Dec '14 – 6M)*

39. The input to the full wave rectifier is $v(t) = 200 \sin 50t$. If R_L is 1kΩ and forward resistance of diode is 50Ω, find:
    i) D.C current through the circuit
    ii) The A.C (rms) value of current through the circuit
    iii) The D.C output voltage
    iv) The A.C power input
    v) The D.C power output
    vi) Rectifier efficiency. *(MQP '15 – 6M)*

40. In a full wave rectifier, the input is from $30 - 0 - 30$ V transformer. The load and diode forward resistances are $100\,\Omega$ and $10\,\Omega$ respectively. Calculate the average voltage, dc output power, ac input power, rectification efficiency and percentage regulation. *(MQP '14 – 5M)*

41. The input voltage applied to the primary of a 4:1 step down transformer of a full wave centre tap rectifier is 230 V, 50 Hz. If the load resistance is $600\,\Omega$ and forward resistance is $20\,\Omega$, determine the following:
    i) dc output power
    ii) Rectification efficiency
    iii) PIV *(Dec '17 – 6M)*
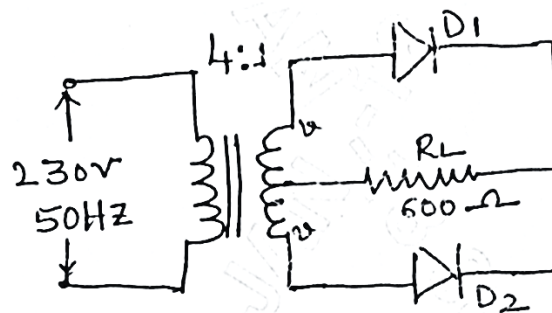
42. A 4.3V Zener diode is connected in series with 820 Ω resistor and DC supply voltage of 12V. Find the diode current and the power dissipation. *(Jun '16 – 5M)*

43. For a Zener regulator shown in the figure, calculate the range of input voltage for which output will remain constant.
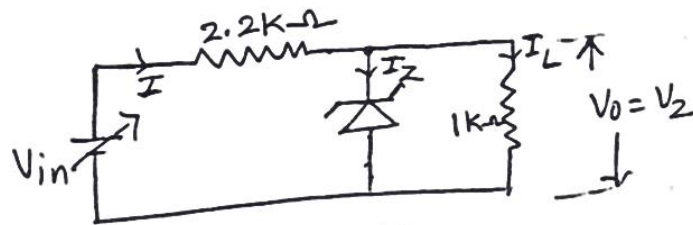
$V_Z = 6.1V$, $I_{Zmin} = 2.5mA$, $I_{Zmax} = 25mA$, $r_Z = 0\Omega$.   *(Jun '16 – 4M)*

44. Design Zener voltage regulator for the following specifications:
    Input Voltage $= 10V \pm 20\%$, Output Voltage $= 5V$, $I_L = 20mA$, $I_{Zmin} = 5mA$ and $I_{Zmax} = 80mA$.   *(MQP '14 – 5M)*

Bipolar Junction Transistors (BJTs)

1. With a neat diagram, explain the operation of an NPN transistor.   *(Dec '17, Jun '16 – 5M)*

2. With a neat diagram, explain the operation of a PNP transistor.   *(Dec '17)*

3. With neat diagrams, explain the operation of PNP and NPN transistors.   *(Dec '17 – 8M)*

4. Draw a sketch to show the various currents in an NPN transistor / a PNP transistor and deduce the relationship between various components.

5. Derive an equation for the collector current of a PNP transistor in terms of base current and α_{dc}.   *(Dec '14 – 5M)*

6. Derive the relation between the α_{dc} and β_{dc} of a transistor.
   (Dec '17, Jun '17 – 4M, Dec '16, Jun '16, Dec '14, MQP '15)

7. Explain voltage and current amplification using transistor.

8. Considering NPN transistor in common emitter configuration, explain how it acts as voltage amplifier.   *(Dec '15 – 6M)*

9. What are the three transistor configurations? Compare and contrast the characteristics of these configurations. State any one application of each of these configurations.
   (Jun '16 – 6M)

10. With a neat diagram, explain the input, output and current gain characteristics of a transistor in *common base* (CB) configuration.   *(Dec '17 – 5M, Dec '16 – 7M)*

11. Explain briefly the common emitter circuit. Explain the input, output and current gain characteristics of a transistor in *common emitter* (CE) configuration. Also explain active region, cut off region and saturation region by indicating them on the characteristic curve.
    (Dec '17 – 7M, Jun '17 – 8M, Dec '16 – 8M, Jun '16 – 6M, Dec '15 – 8M, Dec '14 – 7M, MQP '15 – 4M, MQP '14 – 7M)

12. With a neat diagram, explain the input, output and current gain characteristics of a transistor in *common collector* configuration.

13. Calculate I_C, I_E and β_{dc} for a transistor that has $\alpha_{dc} = 0.98$ and $I_B = 100\mu A$.
    (Dec '17 – 6M, MQP '15 – 4M)

14. Calculate the value of I_C for a transistor that has $\alpha = 0.98$ and $I_B = 200\mu A$. *(Jun '17 – 4M)*

15. In a common base transistor circuit if $\alpha = 0.99$ and $I_C = 5mA$, compute the values of β and I_B. ***(Jun '17 – 4M)***

16. Find I_C and I_E for a transistor, given that $\alpha_{dc} = 0.96$ and $I_B = 110\mu A$. Also calculate the β_{dc} of the transistor. ***(Dec '16 – 5M)***

17. Find the values of β, α and I_E for a transistor which has $I_B = 100\mu A$ and $I_C = 2mA$. ***(Dec '16 – 4M, Jun '16 – 5M)***

18. Find α_{dc}, I_B and β_{dc} for transistor with $I_C = 2.5mA$ and $I_E = 2.55mA$. ***(Jun '16 – 3M)***

19. In a common emitter transistor circuit, if $\beta = 100$ and $I_B = 50\mu A$, compute the values of α, I_E and I_C. ***(Dec '15 – 5M, MQP '14 – 5M)***

20. Calculate the values of I_C and I_E for a BJT with $\alpha_{dc} = 0.97$ and $I_B = 50\mu A$. Determine β_{dc}. ***(Dec '15 – 4M)***

21. Calculate the value of I_C, I_E and β_{dc} for a transistor with $\alpha = 0.98$ and $I_B = 120\mu A$. ***(Jun '15 – 6M)***

Module – 2
BJT Biasing

1. What is the need for transistor biasing? ***(Jun '16)***

2. What is a DC load line? Explain with a fixed bias (base bias) circuit diagram. Also explain the importance of the bias point/Q-point/operating point. ***(MQP '15 – 5M)***

3. With a neat diagram and necessary equations, explain the operation of a base bias (fixed bias) circuit using NPN transistor.
(Dec '17 – 6M, Jun '17 – 4M, Dec '16 – 5M, Dec '14 – 7M, MQP '15)

4. What is DC load line? With neat circuit diagram and necessary equations, explain the operation of collector to base bias circuit. ***(Dec '17 – 5M)***

5. What is DC load line? With neat circuit diagram and necessary equations, explain the operation of voltage divider bias circuit. ***(Dec '17 – 6M, Jun '17 – 8M, Dec '16 – 8M)***

6. With a neat diagram and equations, explain the operation of a voltage divider bias circuit for an NPN transistor using approximate analysis. ***(Jun '16 – 8M, MQP '15 – 5M)***

7. With a neat diagram and equations, explain the operation of a voltage divider bias circuit using accurate/precise/exact analysis.
(Jun '17 – 8M, Jun '16, Dec '15 – 10M, MQP '14 – 8M)

8. Mention the advantages of voltage divider bias. ***(Dec '15)***

9. For the base bias circuit, $V_{CC} = 18$ V, $R_C = 2.2$ kΩ, $R_B = 470$ kΩ, $h_{FE} = 100$ and $V_{BE} = 0.7$ V. Find I_B, I_C and V_{CE}. Draw the DC load line and indicate the Q-point.
(Dec '17 – 6M, Dec '15 – 8M, Jun '15 – 8M)

10. A fixed bias circuit has $V_{CC} = 10$ V, $R_B = 220$ kΩ, $R_C = 1.2$ kΩ and $\beta = 50$. Draw DC load line and mark Q-point. ***(Dec '16 – 6M)***

11. For the circuit shown in the figure, find the Q-point values and draw DC load line, where $V_{BE} = 0.7$ V and $\beta = 50$. ***(Jun '16 – 6M)***
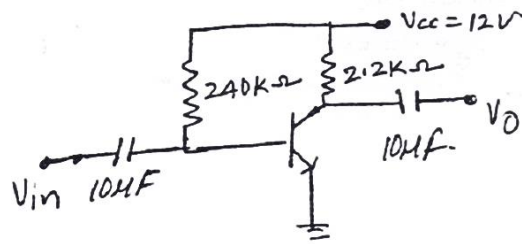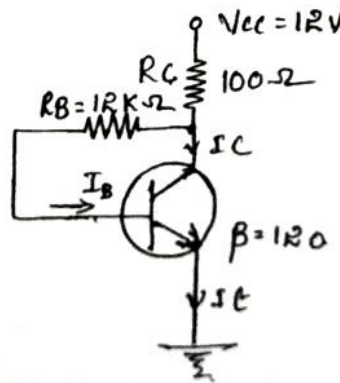
12. Determine the operating point for a silicon transistor biased by base bias method with $\beta = 100$, $R_B = 500$ kΩ, $R_C = 2.5$ kΩ and $V_{CC} = 20$ V. Also draw the DC load line.

    (MQP '14 – 6M)

13. For the circuit shown in figure, compute
    i) Three transistor currents
    ii) Voltage drop across R_C and R_B *(Dec '16 – 5M)*

14. Accurately analyse the voltage divider bias circuit which has $V_{CC} = 18$ V, $R_1 = 33$ kΩ, $R_2 = 12$ kΩ, $R_C = 1.2$ kΩ and $R_E = 1$ kΩ. Determine V_E, V_C, V_{CE}, I_C and Q-point when transistor $h_{FE} = 200$.   *(Dec '17 – 8M)*

15. In a voltage divider bias circuit, $V_{CC} = 24$ V, $R_1 = 180$ kΩ, $R_2 = 56$ kΩ, $R_E = 4.7$ kΩ and $R_C = 8.2$ kΩ. Calculate the approximate levels of I_C, V_E, V_C and V_{CE}.   *(Dec '17 – 5M)*

16. A voltage divider bias circuit has $V_{CC} = 15$ V, $R_C = 2.7$ kΩ, $R_E = 2.2$ kΩ, $R_1 = 22$ kΩ, $R_2 = 12$ kΩ and $h_{FE} = 50$. Calculate V_E, V_C, I_C and V_{CE} and also draw DC load line and mark the Q-point. Assume $V_{BE} = 0.7$ V.   *(Dec '14 – 8M)*

17. A base bias circuit with $V_{CC} = 18$ V uses a transistor with $V_{BE} = 0.7$ V. The circuit is to have $V_{CE} = 9$V and $I_C = 2$mA. Plot the Q-point. Determine the required value of R_C.

    (Jun '16 – 5M)

18. A base bias circuit with a 12 V supply uses a transistor with $h_{FE} = 70$. Design the circuit so that $I_C = 2$ mA and $V_{CE} = 9$ V (Assume $R_E = 0$).   *(Dec '15 – 6M)*

19. Design the voltage divider bias circuit to operate from 12 V supply. The bias conditions are $V_{CE} = 3$ V, $V_E = 5$ V, and $I_C = 1$ mA. Assume $V_{BE} = 0.7$ V.   *(Jun '15 – 7M, MQP '15 – 5M)*

Introduction to Operational Amplifiers

1. What is an Op-Amp? Mention the applications of Op-Amp.

    (Dec '17, Dec '16, Dec '15, MQP '15, MQP '14)

2. Explain the block diagram of an operational amplifier.   *(Jun '16)*

3. Define the following parameters of an Op-Amp: (i) Differential gain (ii) Common mode gain (iii) CMRR (iv) PSRR (v) Slew rate.   *(Dec '17 – 5M, Jun '16 – 5M, Dec '15 – 6M)*

4. Explain the characteristics of an ideal Op-amp.
(Dec '17 – 6M, Jun '17 – 4M, Dec '16 – 6M, Jun '16 – 7M, Dec '15 – 4M, Jun '15 – 6M, Dec '14 – 5M, MQP '15, MQP '14 – 6M)

5. Write a short note on virtual ground concept of an Op-Amp.   *(Dec '17 – 6M)*

6. Explain the operation of an Op-Amp as an (i) Inverting amplifier (ii) Non inverting amplifier. Derive an expression for the output voltage.
(Dec '17 – 4M, Jun '17 – 6M, Dec '16 – 6M, Jun '16 – 5M)

7. Draw the circuit of inverting Op-Amp. Derive the expression for the voltage gain.
(Dec '17 – 5M)

8. With neat circuit and necessary equations, explain the voltage follower circuit using operational amplifier. Mention its important properties.
(Dec '17, Jun '17 – 6M, Dec '16 – 6M, Dec '15 – 4M, Jun '15 – 5M, MQP '15 – 6M, MQP '14)

9. Explain how an Op-Amp can be used as (i) Inverting summer (ii) Non inverting summer.
(Dec '17, Jun '17, MQP '14)

10. Derive the expression for the output of a three input summing amplifier.
(Dec '17 – 5M, Dec '15 – 5M, MQP '15 – 5M)

11. Show with a circuit diagram, how an Op-Amp can be used as a subtractor.   *(Dec '16 – 8M)*

12. With a neat circuit diagram, show how an Op-Amp can be used as an integrator. Derive the expression for output voltage.
(Dec '17 – 4M, Jun '17 – 4M, Dec '16, Jun '16 – 6M, Dec '15 – 6M, MQP '14)

13. With a neat circuit diagram, show how an Op-Amp can be used as a differentiator. Derive the expression for output voltage.   *(Dec '17, Dec '16, Dec '14 – 5M)*

14. An Op-Amp has an open loop voltage gain of 10^4 and a common mode voltage gain of 0.1. Express the CMRR in dB.   *(Jun '16 – 8M)*

15. Find the gain of a non-inverting amplifier if $R_f = 10 \text{ k}\Omega$ and $R_1 = 1 \text{ k}\Omega$.   *(Dec '15 – 6M)*

16. Design an inverting and non inverting operational amplifier to have a gain of 15.
(Dec '17 – 5M)

17. Calculate the output voltage of a three input inverting summing amplifier, given $R_1 = 200 \text{ k}\Omega$, $R_2 = 250 \text{ k}\Omega$, $R_3 = 500 \text{ k}\Omega$, $R_f = 1 \text{ M}\Omega$, $V_1 = -2V$, $V_2 = -1V$ and $V_3 = +3V$.
(Jun '16 – 4M)

18. Design an adder using Op-Amp to give the output voltage $V_o = -[2V_1 + 3V_2 + 5V_3]$.
(Dec '17 – 6M)

19. Design an Op-Amp circuit that will produce an output equal to $-[4V_1 + V_2 + 0.1V_3]$.
(Dec '17 – 6M)

20. Design an inverting summing circuit with feedback $R_f = 100 \text{ k}\Omega$ using an Op-Amp to generate the output $V_o = -[3V_1 + 4V_2 + 5V_3]$.   *(Dec '16 – 6M)*

21. Design an adder circuit using Op-Amp to obtain an output voltage of $V_o = -[0.1V_1 + 0.5V_2 + 2V_3]$, where V_1, V_2 and V_3 are input voltages. Draw the circuit diagram. *(Jun '15 – 8M)*

22. Find the output of the following Op-Amp circuit.
(Jun '17 – 5M, Dec '16 – 5M, MQP '14 – 5M)
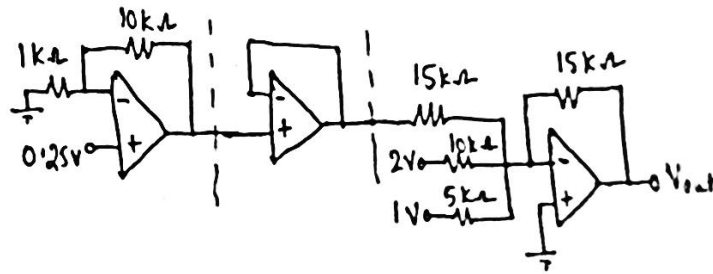
23. Find the output of the following Op-Amp circuit. *(Jun '17 – 5M)*
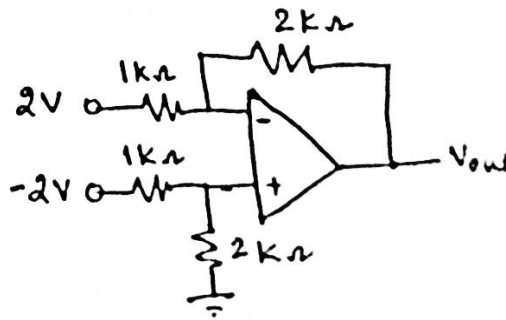
24. Determine V_o for the circuit shown below. *(Jun '16 – 5M)*
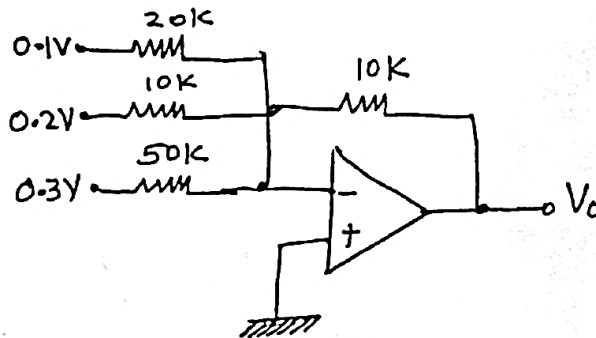
25. For the circuit shown in the figure, calculate the output voltage. *(Dec '15 – 4M)*
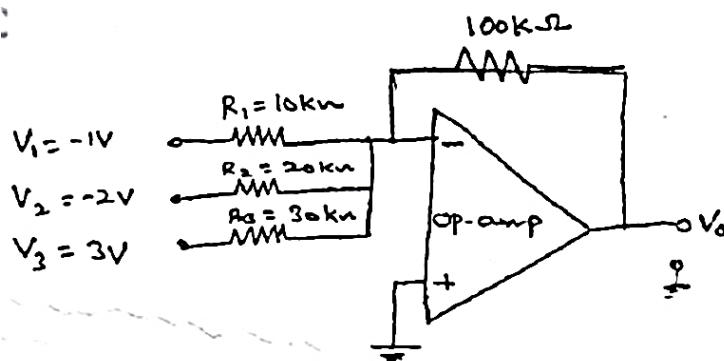
26. Write expression for output voltage at points A, B, C, D and E as shown in figure.

(Dec '14 – 10M)
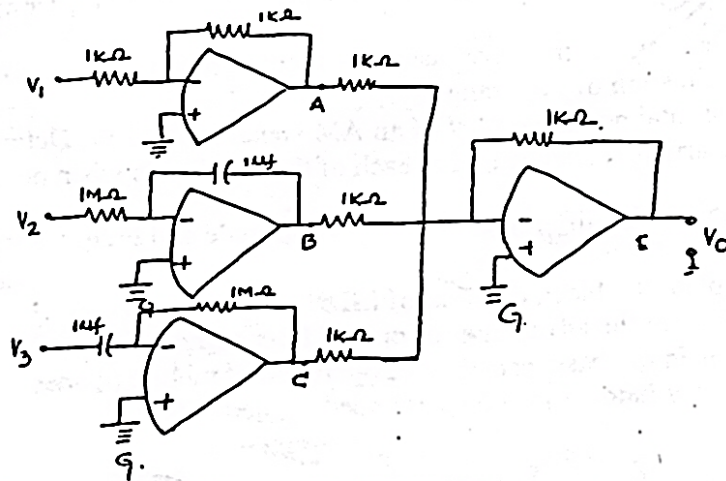
27. Find the output of the following Op-Amp Circuit   *(MQP '14 – 5M)*
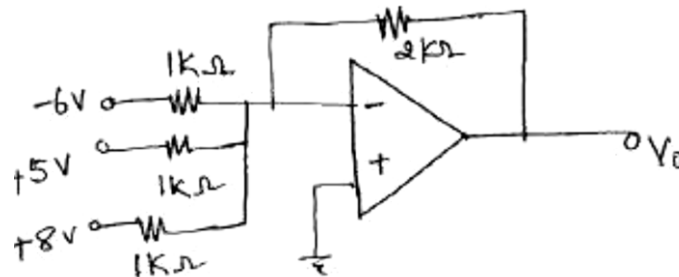
Module – 3
Digital Electronics

1. What is digital logic? With a diagram, show the switching and logic levels in a digital waveform.

2. What is Boolean algebra? State the laws of Boolean algebra.

3. State and prove DeMorgan's theorem for (i) 2 variables (ii) 3 variables (iii) 4 variables.
   (Dec '17 – 8M, Jun '17 – 6M, Dec '16 – 5M, Jun '16 – 4M, Dec '15 – 6M, Jun '15 – 6M, Dec '14 – 6M, MQP '15 – 8M, MQP '14 – 4M)

4. With the help of switching circuit, input/output waveforms and truth table, explain the operation of a NOT Gate.   *(MQP '14 – 5M)*

5. Explain the basic gates AND, OR and NOT gates with truth tables.   *(Jun '17 – 6M)*

6. Write symbol and truth tables of AND, OR, EX-OR and NOT gates.   *(Jun '17 – 8M)*

7. With the help of a diode switching circuit and truth table, explain the operation of (i) OR gate (ii) AND gate.
   (Dec '17 – 6M, Jun '16 – 8M, Dec '15 – 4M, Jun '15 – 6M, Dec '14 – 4M)

8. Explain the operation of (i) NOR gate (ii) NAND gate (iii) XOR gate (iv) XNOR gate.

9. Write the symbol, truth table and final expression for NAND and EX-OR gate (for two inputs).
   (Jun '16 – 4M)

10. Design a logic circuit, symbol and truth table of exclusive – OR gate. *(Dec '14 – 4M)*

11. What are universal gates? Realize AND and OR gates using universal gates.
    (Dec '16 – 5M, Dec '15 – 2M, Jun '15 – 5M)

12. What is the speciality of NAND and NOR gates? Realize basic gates using (i) NAND gates only (ii) NOR gates only. *(Jun '17 – 4M, Jun '16 – 5M, Dec '14 – 4M)*

13. Realize two input Ex-OR gate using only NAND gates. *(Dec '15 – 5M, MQP '14 – 5M)*

14. Realize a two input exclusive NOR gate using only NAND gates, indicating the output at each of the gate. *(Dec '17 – 4M)*

15. Implement Ex-OR gate using only NOR gates. *(Dec '16 – 5M)*

16. Explain the half adder circuit. *(Jun '17 – 4M)*

17. Design a half adder circuit and implement it using logic gates.

18. Realize a half adder using (i) NAND gates only (ii) NOR gates only.
    (Jun '16 – 4M, MQP '15 – 5M)

19. Explain the full adder circuit. *(Jun '17 – 6M, MQP '15 – 5M)*

20. Explain the full adder circuit with truth table. Realize the circuit for sum and carry using logic gates (basic gates). *(Dec '17 – 8M, Dec '16 – 8M, Dec '15 – 7M, Jun '15 – 8M)*

21. Design a full adder and implement it using two half adders and write the equations for sum and carry.
    (Dec '17 – 8M, Jun '17 – 8M, Dec '16 – 5M, Jun '16 – 7M, Dec '15, Dec '14 – 6M, MQP '14 – 6M)

22. Realize a full adder using (i) NAND gates only (ii) NOR gates only. *(Jun '15)*

23. Design a logic circuit using basic gates with three inputs A, B, C and output Y that goes low only when A is high and B and C are different. *(MQP '14 – 5M)*

24. Convert:
    i) $(172.625)_{10} = (?)_{16} = (?)_2$
    ii) $(BCDE)_{16} = (?)_2 = (?)_8$
    iii) $(10111101.0110)_2 = (?)_{10} = (?)_{16}$ *(Dec '17 – 6M)*

25. Convert:
    i) $(2AD.E3)_{16}$ to its octal and decimal equivalents.
    ii) $(1456.72)_8$ to its decimal and hexadecimal equivalents. *(Dec '17 – 4M)*

26. Convert the following:
    i) $(49.5)_{10} = (?)_{16}$
    ii) $(1062.403)_8 = (?)_{10}$
    iii) $(642.71)_8 = (?)_2$ *(Jun '17 – 6M)*

27. Convert:
    i) $(655.70)_8 = (?)_{10} = (?)_{16}$

ii) $(238.20)_{10} = (?)_8 = (?)_2$ *(Jun '17 – 8M)*

28. Convert $(1101101)_2 = (?)_{10}$ and $(96)_{10} = (?)_2$.   *(Dec '16 – 4M)*

29. Convert $(FA876)_{16} = (?)_8$ and $(237)_8 = (?)_{16}$.   *(Dec '16 – 4M)*

30. Convert:
    i) $(1010101)_2 = (?)_{10} = (?)_8$
    ii) $(ABCD)_{16} = (?)_2 = (?)_8$ *(Dec '16 – 5M)*

31. Convert:
    i) $(526.44)_8 = (?)_2 = (?)_{10}$
    ii) $(48350)_{10} = (?)_{16} = (?)_8$ *(Jun '16 – 4M)*

32. Convert:
    i) $(342.56)_{10} = (?)_2 = (?)_8$
    ii) $(BCDE) = (?)_2 = (?)_8$ *(Jun '16 – 4M)*

33. i) Convert A6B.F5 to binary
    ii) Convert binary 110.111 into decimal equivalent   *(Jun '16 – 6M)*

34. Convert the following:
    (i) $(172.625)_{10} = (?)_2$ (ii) $(ABCD.72)_{16} = (?)_8$ (iii) $(10111101.0101)_2 = (?)_{10}$
                                                                                                                                (Dec '15 – 6M)

35. Convert (i) $(35.45)_{10} = (?)_2$ (ii) $(475.25)_8 = (?)_{10}$ (iii) $(3FD)_{16} = (?)_2$
                                                                                                                                (Dec '15 – 6M)

36. Perform the following conversions:
    (i) $(1234.56)_8 = (?)_{10}$ (ii) $(10110101001.101011)_2 = (?)_{16}$ (iii) $(988.86)_{10} = (?)_2$
    (iv) $(532.65)_{10} = (?)_{16}$ (v) $(ABCD.EF)_H = (?)_8$ *(Jun '15 – 5M)*

37. Convert (i) $(294.6875)_{10} = (?)_8$ (ii) $(356.15)_8 = (?)_2 = (?)_{10}$.   *(Dec '14 – 5M)*

38. Convert $(1010111011110101)_2 = (?)_{16}$ and $(FA876)_{16} = (?)_2$.   *(MQP '15 – 4M)*

39. Convert $(1101101)_2 = (?)_{10}$ and $(69)_{10} = (?)_2$.   *(MQP '15 – 4M)*

40. Convert (i) $(1AD.E0)_{16} = (?)_{10} = (?)_8$ (ii) $(356.15)_8 = (?)_2 = (?)_{10}$
                                                                                                                                (MQP '14 – 5M)

41. Perform the following:
    i)   Convert $(57345)_{10} = (?)_{16}$
    ii) Subtract $(28)_{10} - (19)_{10}$ using 2's complement method.   *(Dec '17 – 6M)*
42. Perform the following:
    i)   Convert $(FA27D)_{16} = (?)_2 = (?)_8 = (?)_{10}$
    ii) Subtract $10.0101 - 101.1110$ using 1's complement method.   *(Dec '17 – 6M)*
43. Perform the following:
    i)   Convert $(725.25)_8 = (?)_{10} = (?)_2$
    ii) Subtract using 2's complement $(4 - 9)_{10}$
    iii) $(11010.101)_2 = (?)_8 = (?)_{16}$ *(Dec '17 – 6M)*

44. Subtract $(1111.101)_2$ from $(1001.101)_2$ using 1's and 2's complement method.
                                                                                                                                (Dec '17 – 6M, MQP '14)

45. Perform the following:
    i) $(11010)_2 - (10111)_2$ using 1's complement method
    ii) $(111001)_2 - (101011)_2$ using 2's complement method   *(Jun '17 – 8M)*

46. Subtract $(111001)_2$ from $(101011)_2$ using 2's complement method.
                                            (Dec '16 – 5M, Jun '16)

47. Subtract $(19)_{10}$ from $(15)_{10}$ using 1's and 2's complement methods.   *(Dec '16 – 6M)*

48. Subtract $(101011)_2$ from $(111001)_2$ using 2's complement method.   *(Jun '16 – 4M)*

49. Perform the subtraction:
    i) $(11010)_2 - (10000)_2$ using 1's complement
    ii) $(1000100)_2 - (1010100)_2$ using 2's complement   *(Jun '16 – 4M)*

50. Perform the subtraction with the following binary numbers using 1's and 2's complement
    method: (i) $11010 - 1101$ (ii) $10010 - 10011$ *(Jun '16 – 6M)*

51. Perform the following operations using 1's and 2's complement technique:
    (i) $(56)_{10} - (79)_{10}$ (ii) $(23)_{10} - (18)_{10}$ *(Dec '15 – 6M)*

52. Subtract $(111001)_2$ from $(101011)_2$ using 2's complement method.   *(Dec '15 – 4M)*

53. i) Subtract $(1000.01)_2$ from $(1011.10)_2$ using 1's and 2's complement method.
    ii) Add $(7AB.67)_{16}$ with $(15C.71)_{16}$ *(Jun '15 – 5M)*

54. Subtract $(111)_2$ from $(1010)_2$ using 1's and 2's complement method.   *(Dec '14 – 5M)*

55. Subtract $(11101.111)_2$ from $(11111.101)_2$ using 2's complement method.
                                            (MQP '14 – 5M)

56. Simplify the Boolean function $F = \overline{A}BC + A\overline{B}C + ABC$.   *(Jun '17 – 4M)*

57. Prove the following Boolean identity using truth table:
    (i) $A + AB = A$ (ii) $A + \overline{A}B = A + B$ *(Jun '16 – 4M)*

58. Show that:
    i) $A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C = B + C$
    ii) $\overline{\overline{AB} + \overline{A} + AB} = 0$
    iii) $AB + A(B + C) + B(B + C) = B + AC$ *(Dec '15 – 6M)*

59. Simplify the Boolean expression: $\overline{\overline{xy + xy\overline{z}} + x(y + x\overline{y})}$.   *(Dec '17 – 4M)*

60. Factorise the following Boolean equations: $Y_1 = A\overline{B} + AB$, $Y_2 = (B + CA)(C + \overline{A}B)$.
                                            (MQP '15 – 6M)

61. Simplify $Y = AB + \overline{AC} + A\overline{B}C(AB + C)$.   *(MQP '14 – 5M)*

62. Simplify the expression and realize using basic gates: $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C}$.
                                            (Dec '17 – 5M)

63. Simplify and realize the expression using basic gates: $Y = \overline{AB} + \overline{AC} + A\,\overline{B}\,\overline{C} + \overline{AB + C}$.
                                            (Dec '17 – 6M)

64. Simplify and realize using basic gates: $\overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y}\,Z + \overline{X}\,Y + X\,\overline{Y}$.   *(Dec '16 – 5M)*

65. Simplify the following expression and realize using basic gates: $Y = A(\overline{ABC} + A\overline{B}C)$.

                                                      (Jun '16 – 4M)

66. Simplify $Y = AB + ABC + \overline{A}B + A\overline{B}C$ and construct logic circuit.   ***(Jun '16 – 4M)***

67. Simplify and realize using basic gates:
    i) $ABC + A\overline{B}C + AB\overline{C} + \overline{A}BC$
    ii) $(\overline{A + B})(\overline{A} + \overline{C})(\overline{B} + C)$ ***(Dec '14 – 6M)***

68. Realize $Y = AB + CD + E$ using NAND gates.   ***(Dec '17 – 6M)***

69. Simplify the given Boolean equation $Y = (A + \overline{B})(CD + E)$ and realize using NAND gates only.   ***(Jun '17 – 4M)***

70. Simplify and realize the following using NAND gates only: $A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B} + \overline{A}\,\overline{C}$.   ***(Dec '16 – 5M)***

71. Realize the following using only NAND gates: $Y = (A + \overline{B} + C) \cdot (\overline{A} + B + C)$. ***(Dec '16 – 5M)***

72. Simplify and realize the Boolean expression using two input NAND gates only:

     $(A + \overline{B} + C)(\overline{A} + B + C)$.   ***(Dec '17 – 5M)***

73. Simplify $Y = A + \overline{A}B + AB\overline{C}$ and implement using logic gates and NOR gates. ***(Dec '17 – 6M)***

74. Simplify and realize the following expressions using only NAND and NOR:
    (i) $Y = (A + \overline{B})(B + C)(\overline{C} + \overline{B})$ (ii) $Y = AB + AC + BD + CD$ ***(Dec '15 – 10M)***

Module – 4
Flip-Flops

1. What is a flip-flop? Distinguish between a latch and a flip-flop.
         (Dec '17 – 4M, Jun '17 – 4M, Dec '16 – 2M, Jun '16, Dec '15, Jun '15 – 4M, MQP '14 – 4M)

2. What is a latch?   ***(Dec '17)***

3. With a logic diagram and truth table, explain the operation of NAND gate latch.
                                       (Dec '17 – 10M, Jun '17 – 8M, Jun '16 – 5M)

4. With a logic diagram and truth table, explain the operation of NOR gate latch.
                       (Dec '17, Dec '16 – 5M, Jun '16 – 8M, Dec '15 – 6M, MQP '14 – 6M)

5. What is RS flip-flop? Explain its operation with circuit diagram, logic symbol and truth table.
           (Dec '17 – 6M, Jun '17 – 8M, Jun '16 – 5M, Dec '15 – 5M, Jun '15 – 6M, MQP '15 – 6M)

6. With a logic diagram and truth table, explain the operation of a clocked (or gated) RS flip-flop using NAND gates.
    (Dec '17 – 8M, Jun '17 – 8M, Dec '16 – 8M, Jun '16 – 5M, Dec '15 – 8M, Dec '14 – 6M, MQP '15 - 4M, MQP '14 – 5M)

7. Draw the traditional and IEEE logic symbols of AND, OR, NOT, NAND, NOR, XOR and XNOR.
                                                         (MQP '15 – 4M)

Microcontrollers

1. Define microcontrollers. Write their important applications.   ***(Dec '16 – 5M)***

2. List the differences between microprocessor and microcontroller.
    (Dec '17 – 4M, Jun '17 – 8M, Jun '16 – 5M, Dec '15 – 5M, Jun '15 – 8M, MQP '14 – 5M)

3. List the features of 8051 microcontroller.   ***(Jun '16 – 5M)***

4. With a neat block diagram, explain the architecture of 8051 microcontroller.

    (Dec '17 – 10M, Jun '17 – 8M, Dec '16 – 8M, Jun '15 – 6M, Dec '15 – 10M, Dec '14 – 9M, MQP '15 – 6M)

5. Explain flag register of 8051 microcontroller.   ***(Dec '16 – 5M)***

6. Explain the logic pinout and signals of 8051 microcontroller.

7. What is stepper motor? With a neat block diagram, explain the working principle of microcontroller based stepper motor control system.
    (Dec '17 – 10M, Jun '17 – 8M, Dec '16 – 6M, Jun '16 - 8M, Dec '15 – 8M, MQP '15 – 6M)

Module – 5
Communication Systems

1. Define communication.   ***(Dec '17)***

2. With a neat block diagram, explain the elements of communication system.
    (Dec '17 – 6M, Jun '17 – 6M, Dec '16 – 5M, Jun '16 – 6M, MQP '15 – 5M)

3. What are commonly used frequency ranges in communication system? Mention the application of each range.   ***(Dec '17 – 4M, Dec '14 – 5M, MQP '14 – 4M)***

4. What is modulation? Explain the need for modulation. List the different types of modulation schemes.   ***(Jun '17 – 4M, Jun '16 – 5M, Dec '15 – 5M, Jun '15 - 6M, Dec '14 – 4M)***

5. What is amplitude modulation? Explain with neat waveforms and derive the expression for the AM wave. Also draw the frequency spectrum.
    (Dec '17 – 8M, Jun '17 – 8M, Dec '16 – 6M, Jun '16 – 5M, Dec '15 – 8M, Jun '15 – 8M, Dec '14, MQP '15 – 5M, MQP '14)

6. Define amplitude modulation. Draw the AM signal and its spectrum. For an amplitude modulated wave, prove that total power is given by $P_t = P_c \left[1 + \frac{\mu^2}{2} \right]$, where μ is the modulation index.   ***(Dec '17 – 6M)***

7. Define modulation index. Obtain the expression for modulation index of AM wave in terms of V_{max} and V_{min}.   ***(Dec '15)***

8. Derive an expression for modulation index in AM.   ***(Dec '16 – 6M)***

9. Derive the expression for the total power transmitted in an AM wave.
    (Jun '17, Dec '14 – 5M, MQP '14 – 6M)

10. With a neat diagram, explain demodulation (detection) of an AM wave.
    (Jun '17 – 4M, Jun '16 – 5M)

11. Explain frequency modulation with neat waveforms.
    (Jun '17 – 6M, Dec '16 – 5M, Dec '15 – 8M, MQP '15 – 5M)

12. Mention the advantages of frequency modulation.   ***(Jun '16 - 5M)***

13. Differentiate between amplitude modulation and frequency modulation.
    (Dec '17 – 6M, Jun '17 – 4M, Dec '16 – 5M, Dec '15 – 4M, Jun '15 – 8M, Dec '15 – 5M, MQP '15 – 6M, MQP '14 – 4M)

14. A carrier of 10 V peak and frequency 100 kHz is amplitude modulated by a sine wave of 4 V and frequency 1000 kHz. Determine the modulation index for the modulated wave and draw the amplitude spectrum.   ***(Dec '16 – 6M)***

15. An audio frequency signal $5 \sin 2\pi(1000)t$ is used to amplitude modulate a carrier of $100 \sin 2\pi(10^6)t$. Assume modulation index of 0.4. Find
    i)   Sideband frequencies
    ii) Bandwidth required
    iii) Amplitude of each sideband
    iv) Total power delivered to a load of 100Ω   ***(Dec '17 – 6M)***

16. An audio frequency signal $10 \sin(2\pi \times 500)t$ is used to amplitude modulate a carrier of $50 \sin(2\pi \times 10^5)t$. Calculate
    i)   Modulation index
    ii) Sideband frequencies
    iii) Bandwidth
    iv) Amplitude of each sideband
    v)   Total power delivered to a load of 600Ω
    vi) Transmission efficiency   ***(Dec '16 – 8M, Jun '15 – 6M)***

17. A carrier of 1 MHz, with 400 W of its power is amplitude modulated with a sinusoidal signal of 2500 Hz. The depth of modulation is 75%. Calculate the sideband frequencies, the bandwidth, the power in the sidebands and the total power in the modulated wave.
    (Jun '16 – 5M)

18. A 1 MHz carrier is amplitude modulated by a 40 kHz modulating signal with a modulation index of 0.5. The unmodulated carrier is having a power of 1 kW. Calculate the power of the amplitude modulated signal. Also find the sideband frequencies.   ***(Jun '16 – 5M)***

19. A 500 W, 1 MHz carrier is amplitude modulated with a sinusoidal signal of 1 kHz. The depth of modulation is 60%. Calculate the bandwidth, power in the sidebands and the total power transmitted.   ***(Dec '15 - 7M)***

20. The total power content of an AM signal is 1000 W. Determine the power being transmitted at carrier frequency and at each of the sidebands when percentage modulation is 100%.
    (Dec '14 – 5M)

21. A 500 W, 100 kHz carrier is modulated to depth of 60% by modulating signal of frequency 1 kHz. Calculate the total power transmitted. What are the side band components of the AM wave?   ***(MQP '15 - 6M)***

22. Calculate the percentage power saving when one side band and carrier is suppressed in an AM signal with modulation index equal to 1.   ***(MQP '14 - 5M)***

23. If an FM wave is represented by the equation $V = 10 \sin(8 \times 10^8 + 4 \sin 1000t)$, calculate
    i) Carrier frequency
    ii) Modulating frequency
    iii) Modulation index
    iv) Bandwidth   *(Dec '17 – 6M)*

24. A 15 kHz audio signal is used to frequency modulate a 100 MHz carrier, causing deviation of 75 kHz. Determine modulation index and bandwidth of the FM signal.   *(Dec '16 – 4M)*

Transducers

1. What is a transducer? Mention any four characteristics a transducer should possess.
    (Dec '17, Jun '17, Jun '16 – 2M, Dec '15 – 2M, Dec '14, MQP '14)

2. Write a note on classification of transducers.

3. Distinguish between active and passive transducers.
    (Dec '17 – 6M, Jun '17 – 4M, Dec '16 – 5M, Dec '15 – 5M, Dec '14 – 6M, MQP '14 – 5M)

4. What is a transducer? Mention four important parameters of an electrical transducer.
    (Dec '17 – 4M)

5. Explain the construction and principle of operation of resistive thermometer (RTD).
    (Dec '17 – 5M, Dec '16 – 5M)

6. Write a note on thermistor. Explain its advantages and limitations. Mention its applications.
    (Dec '17 – 5M, Dec '15 – 6M, Dec '14 – 5M)

7. Explain the construction and the principle of operation of LVDT. Mention its applications.
    (Dec '17 – 6M, Jun '17 – 6M, Dec '16 – 5M, Jun '16 – 6M, Dec '15 – 8M, Jun '15 – 6M, Dec '14 – 6M, MQP '15 – 5M, MQP '14 – 6M)

8. Explain (i) Seebeck effect (ii) Peltier effect (iii) Thompson effect (iv) Hall effect
    (Jun '17 – 6M, Jun '15 – 6M, MQP '14 – 6M)

9. Explain the principle of operation of piezoelectric transducers.
    (Dec '17 – 4M, Jun '17, Jun '16 – 8M)

10. Write a note on photoelectric transducers.   *(Dec '17, Jun '17 – 6M)*

11. Explain the working of photovoltaic transducer.   *(Dec '15 – 8M)*