Flip-Flops

Syllabus: *Flip-Flops: Introduction to Flip-Flops, NAND Gate Latch/ NOR Gate Latch, RS Flip-Flop, Gated Flip-Flops: Clocked RS Flip-Flop.* ***(5 Hours)***

Introduction to Flip-Flops

Digital circuits are classified into two types – Combinational circuits and Sequential circuits. Combinational circuits are the circuits in which the output depends on the present inputs only. Sequential circuits are the circuits in which the output depends on the present input as well as the previous state of the system. The sequential circuits have memory. A flip-flop is the basic element of all sequential systems.

Flip-Flop

A flip-flop is an electronic circuit which has memory. It is a bistable digital circuit, i.e., its outputs have two stable states: logic 1 and logic 0. It is the basic element of all sequential systems.

Difference between Latches and Flip-Flops

Latches and flip-flops are the basic building blocks of the most sequential circuits. The main difference between latches and flip-flops is the method used for changing their state. Latches are controlled by an enable signal and they are level triggered, whereas, flip-flops are controlled by a clock signal and they are edge triggered.

Table 1 Differences between latches and flip-flops

Latches	Flip-Flops
Latches are controlled by an *enable* signal	Flip-flops are controlled by a *clock* signal
Latches are positive or negative level-triggered, i.e., the output changes whenever the enable is 1 (for positive level-triggered) or 0 (for negative level-triggered)	Flip-flops are positive or negative edge-triggered, i.e., the output changes whenever the clock changes from 0 to 1 (for positive edge-triggered) or 1 to 0 (for negative edge-triggered)
Latches are building blocks of sequential circuits and are built from basic gates	Flip-flops are also building blocks of sequential circuits and are built from latches
A latch continuously checks its inputs and changes its output whenever the enable is HIGH	A flip-flop continuously checks its inputs and changes its output only at times determined by the clock signal
The operation of a latch is faster as they do not have to wait for clock signal	Flip-flops are comparatively slower as they have to wait for clock signal

Table 1 summarizes the differences between latches and flip-flops.

Basic Bistable Element

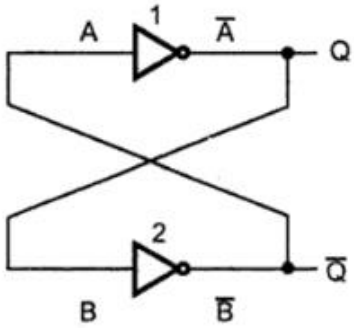


Fig. 1 Basic bistable element

Fig. 1 shows a basic bistable element. It has two inputs and two outputs as shown. The output of one NOT gate is connected to the input of the other. In this case, the outputs Q and $\bar{Q}$ will have a stable value complementary to each other, but cannot be controlled. To control the bistable element, we use latches.

NAND Gate Latch

A NAND gate latch is formed by cross connecting two NAND gates as shown in Fig. 2.

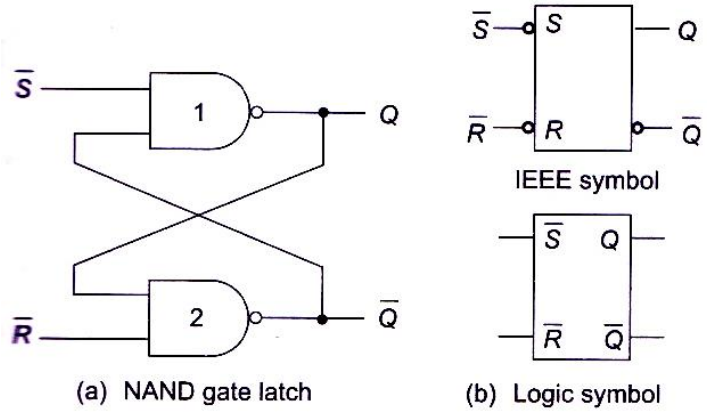


Fig. 2 NAND gate latch

Operation

The inputs are $\bar{R}$ and $\bar{S}$. Hence there are four conditions:

i. **If $\bar{R} = \bar{S} = 1$**

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 1 are (1,1). So its output is $Q = 0$. The inputs to the gate 2 are (0,1). So its output is $\bar{Q} = 1$. (The output does not change).

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are (1,0). So its output is $Q = 1$. The inputs to the gate 2 are (1,1). So its output is $\bar{Q} = 0$. (The output does not change).

*That is, if $\bar{R} = \bar{S} = 1$, there is **no change** in the output.*

ii. If $\bar{R} = 1, \bar{S} = 0$

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 1 are (0,1). So its output is $Q = 1$. The inputs to the gate 2 are (1,1). So its output is $\bar{Q} = 0$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are (0,0). So its output is $Q = 1$. The inputs to the gate 2 are (1,1). So its output is $\bar{Q} = 0$.

*That is, if $\bar{R} = 1, \bar{S} = 0$, the output is **set** ($Q = 1$).*

iii. If $\bar{R} = 0, \bar{S} = 1$

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 1 are (1,1). So its output is $Q = 0$. The inputs to the gate 2 are (0,0). So its output is $\bar{Q} = 1$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 2 are (1,0). So its output is $\bar{Q} = 1$. The inputs to the gate 1 are (1,1). So its output is $Q = 0$.

*That is, if $\bar{R} = 0, \bar{S} = 1$, the output is **reset** ($Q = 0$).*

iv. If $\bar{R} = \bar{S} = 0$

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 1 are (0,1). So its output is $Q = 1$. The inputs to the gate 2 are (1,0). So its output is $\bar{Q} = 1$.

Here $Q = 1$ and $\bar{Q} = 1$, which is not possible. So the output is not valid.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are (0,0). So its output is $Q = 1$. The inputs to the gate 2 are (1,0). So its output is $\bar{Q} = 1$.

Again $Q = 1$ and $\bar{Q} = 1$, which is not possible. So the output is not valid.

*That is, if $\bar{R} = \bar{S} = 0$, the output is not valid. Hence this is **forbidden**.*

Considering all the four cases, the truth table is written as below.

Truth Table:

$\bar{R}$	$\bar{S}$	Q_n	Q_{n+1}	State
1 1	1 1	0 1	0 1	No change
1 1	0 0	0 1	1 1	Set
0 0	1 1	0 1	0 0	Reset
0 0	0 0	0 1	? ?	Forbidden (Illegal)

$\bar{R}$	$\bar{S}$	Q_{n+1}	State
1	1	Q_n	No change
1	0	1	Set
0	1	0	Reset
0	0	?	Forbidden (Illegal)

Q_n - Present state output

Q_{n+1} - Next state output

NOR Gate Latch

A NOR gate latch is formed by cross connecting two NOR gates as shown in Fig. 3.

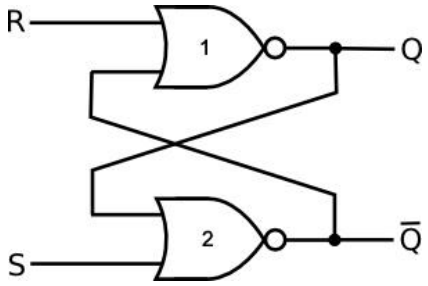


Fig. 3 NOR gate latch

Operation

The inputs are R and S. Hence there are four conditions:

i. If $R = S = 0$

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 1 are (0,1). So its output is $Q = 0$. The inputs to the gate 2 are (0,0). So its output is $\bar{Q} = 1$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are (0,0). So its output is $Q = 1$. The inputs to the gate 2 are (1,0). So its output is $\bar{Q} = 0$.

*That is, if $R = S = 0$, there is **no change** in the output.*

ii. If $R = 0, S = 1$

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 2 are (0,1). So its output is $\bar{Q} = 0$. The inputs to the gate 1 are (0,0). So its output is $Q = 1$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are (0,0). So its output is $Q = 1$. The inputs to the gate 2 are (1,1). So its output is $\bar{Q} = 0$.

*That is, if $R = 0, S = 1$, the output is **set** ($Q = 1$).*

iii. If $R = 1, S = 0$

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 1 are (1,1). So its output is $Q = 0$. The inputs to the gate 2 are (0,0). So its output is $\bar{Q} = 1$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are (1,0). So its output is $Q = 0$. The inputs to the gate 2 are (0,0). So its output is $\bar{Q} = 1$.

*That is, if $R = 1, S = 0$, the output is **reset** ($Q = 0$).*

iv. If $R = S = 1$

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 1 are (1,1). So its output is $Q = 0$. The inputs to the gate 2 are (0,1). So its output is $\bar{Q} = 0$.

Here $Q = 0$ and $\bar{Q} = 0$, which is not possible. So the output is not valid.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 1 are (1,0). So its output is $Q = 0$. The inputs to the gate 2 are (0,1). So its output is $\bar{Q} = 0$.

Again $Q = 0$ and $\bar{Q} = 0$, which is not possible. So the output is not valid.

*That is, if $R = S = 1$, the output is not valid. Hence this is **forbidden**.*

Considering all the four cases, the truth table is written as below.

Truth Table:

R	S	Q_n	Q_{n+1}	State
0 0	0 0	0 1	0 1	No change
0 0	1 1	0 1	1 1	Set
1 1	0 0	0 1	0 0	Reset
1 1	1 1	0 1	? ?	Forbidden (Illegal)

R	S	Q_{n+1}	State
0	0	Q_n	No change
0	1	1	Set
1	0	0	Reset
1	1	?	Forbidden (Illegal)

Q_n - Present state output

Q_{n+1} - Next state output

RS Flip-Flop

In RS flip-flop, the inputs are R and S. We want to achieve $Q = 0$ (Reset) when $R = 1$ and $Q = 1$ (Set) when $S = 1$. Fig. 4 shows the logic diagram and symbol of an RS flip-flop (latch).

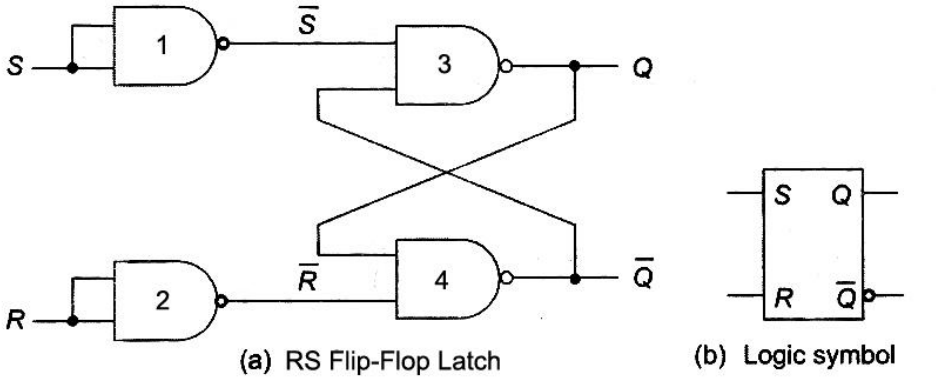


Fig. 4 RS Flip-Flop (Latch)

Operation

The inputs are R and S. NAND gates 1 and 2 act as inverters and produce $\bar{S}$ and $\bar{R}$ respectively which are the inputs to gates 3 and 4. The gates 3 and 4 form a NAND gate latch. The operation can be analyzed for the four conditions:

i. **If $R = S = 0$**

If $R = S = 0$, then $\bar{R} = \bar{S} = 1$.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (1,1). So its output is $Q = 0$. The inputs to the gate 4 are (0,1). So its output is $\bar{Q} = 1$. (The output does not change).

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 3 are (1,0). So its output is $Q = 1$. The inputs to the gate 4 are (1,1). So its output is $\bar{Q} = 0$. (The output does not change).

*That is, if $R = S = 0$, there is **no change** in the output.*

ii. If $R = 0, S = 1$

If $R = 0, S = 1$, then $\bar{R} = 1, \bar{S} = 0$.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (0,1). So its output is $Q = 1$. The inputs to the gate 4 are (1,1). So its output is $\bar{Q} = 0$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 3 are (0,0). So its output is $Q = 1$. The inputs to the gate 4 are (1,1). So its output is $\bar{Q} = 0$.

*That is, if $R = 0, S = 1$, the output is **set** ($Q = 1$).*

iii. If $R = 1, S = 0$

If $R = 1, S = 0$, then $\bar{R} = 0, \bar{S} = 1$.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (1,1). So its output is $Q = 0$. The inputs to the gate 4 are (0,0). So its output is $\bar{Q} = 1$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 4 are (1,0). So its output is $\bar{Q} = 1$. The inputs to the gate 3 are (1,1). So its output is $Q = 0$.

*That is, if $R = 1, S = 0$, the output is **reset** ($Q = 0$).*

iv. If $R = S = 1$

If $R = S = 1$, then $\bar{R} = \bar{S} = 0$.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (0,1). So its output is $Q = 1$. The inputs to the gate 4 are (1,0). So its output is $\bar{Q} = 1$.

Here $Q = 1$ and $\bar{Q} = 1$, which is not possible. So the output is not valid.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 3 are (0,0). So its output is $Q = 1$. The inputs to the gate 4 are (1,0). So its output is $\bar{Q} = 1$.

Again $Q = 1$ and $\bar{Q} = 1$, which is not possible. So the output is not valid.

*That is, if $R = S = 1$, the output is not valid. Hence this is **forbidden**.*

Considering all the four cases, the truth table is written as below.

Truth Table:

R	S	Q_n	Q_{n+1}	State
0 0	0 0	0 1	0 1	No change
0 0	1 1	0 1	1 1	Set
1 1	0 0	0 1	0 0	Reset
1 1	1 1	0 1	? ?	Forbidden (Illegal)

R	S	Q_{n+1}	State
0	0	Q_n	No change
0	1	1	Set
1	0	0	Reset
1	1	?	Forbidden (Illegal)

Q_n - *Present state output*

Q_{n+1} - *Next state output*

Gated Flip-Flops

An RS flip-flop (or latch) is said to be *transparent*, that is, any change in R or S is immediately transmitted to the outputs Q and $\bar{Q}$. If an *enable* or *clock* signal is connected to the NAND gates 1 and 2, we get *Gated Flip-Flops*.

Clocked RS Flip-Flops

In a clocked RS flip-flop, a clock (CLK) signal is fed to the NAND gates 1 and 2 as shown in Fig. 5.

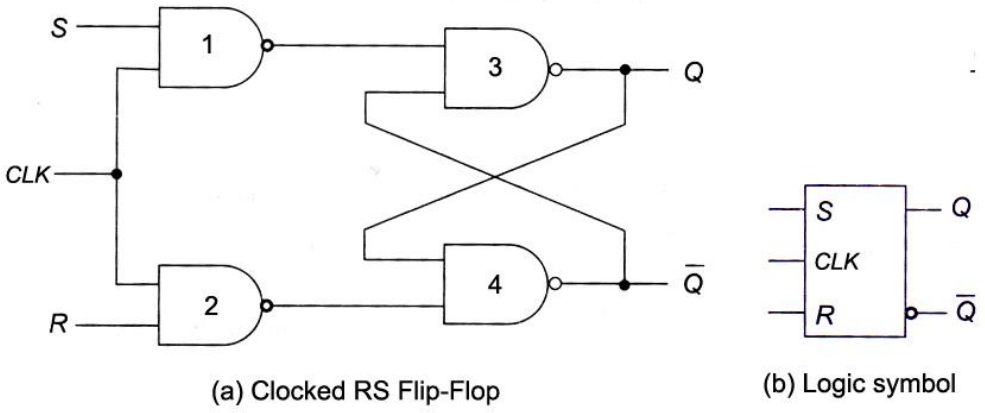


Fig. 5 Clocked RS Flip-Flop (Gated RS Flip-Flop)

Operation

The inputs are R and S. The gates 3 and 4 form a NAND gate latch.

When the clock is HIGH, the outputs of gates 1 and 2 are $\bar{S}$ and $\bar{R}$ respectively. So the latch operates normally.

When the clock is LOW, the output of the gates 1 and 2 are (1,1), which implies that the output does not change and the latch is said to be disabled.

The operation can be analyzed for the following conditions:

i. If $CLK = 1$ and $R = S = 0$

In this case, the outputs of gates 1 and 2 are (1,1) respectively.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (1,1). So its output is $Q = 0$. The inputs to the gate 4 are (0,1). So its output is $\bar{Q} = 1$. (The output does not change).

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 3 are (1,0). So its output is $Q = 1$. The inputs to the gate 4 are (1,1). So its output is $\bar{Q} = 0$. (The output does not change).

*That is, if $CLK = 1$ and $R = S = 0$, there is **no change** in the output.*

ii. If $CLK = 1$ and $R = 0, S = 1$

In this case, the outputs of gates 1 and 2 are (0,1) respectively.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (0,1). So its output is $Q = 1$. The inputs to the gate 4 are (1,1). So its output is $\bar{Q} = 0$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 3 are (0,0). So its output is $Q = 1$. The inputs to the gate 4 are (1,1). So its output is $\bar{Q} = 0$.

*That is, if $CLK = 1$ and $R = 0, S = 1$, the output is **set** ($Q = 1$).*

iii. If $CLK = 1$ and $R = 1, S = 0$

In this case, the outputs of gates 1 and 2 are (1,0) respectively.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (1,1). So its output is $Q = 0$. The inputs to the gate 4 are (0,0). So its output is $\bar{Q} = 1$.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 4 are (1,0). So its output is $\bar{Q} = 1$. The inputs to the gate 3 are (1,1). So its output is $Q = 0$.

*That is, if $CLK = 1$ and $R = 1, S = 0$, the output is **reset** ($Q = 0$).*

iv. If $CLK = 1$ and $R = S = 1$

In this case, the outputs of gates 1 and 2 are (0,0) respectively.

Let the previous state output be $Q = 0$ ($\bar{Q} = 1$). The inputs to the gate 3 are (0,1). So its output is $Q = 1$. The inputs to the gate 4 are (1,0). So its output is $\bar{Q} = 1$.

Here $Q = 1$ and $\bar{Q} = 1$, which is not possible. So the output is not valid.

Let the previous state output be $Q = 1$ ($\bar{Q} = 0$). The inputs to the gate 3 are (0,0). So its output is $Q = 1$. The inputs to the gate 4 are (1,0). So its output is $\bar{Q} = 1$.

Again $Q = 1$ and $\bar{Q} = 1$, which is not possible. So the output is not valid.

*That is, if $CLK = 1$ and $R = S = 1$, the output is not valid. Hence this is **forbidden**.*

v. If $CLK = 0$

In this case, the output of the gates 1 and 2 are (1,1), which implies that the output does not change and the latch is said to be disabled.

Considering all the cases, the truth table is written as below.

Truth Table:

CLK	R	S	Q_n	Q_{n+1}	State
1 1	0 0	0 0	0 1	0 1	No change
1 1	0 0	1 1	0 1	1 1	Set
1 1	1 1	0 0	0 1	0 0	Reset
1 1	1 1	1 1	0 1	? ?	Forbidden (Illegal)
0 0	X X	X X	0 1	0 1	No change

CLK	R	S	Q_{n+1}	State
1	0	0	Q_n	No change
1	0	1	1	Set
1	1	0	0	Reset
1	1	1	?	Forbidden (Illegal)
0	X	X	Q_n	No change

Q_n - Present state output

Q_{n+1} - Next state output

X – Don't care
(May be 0 or 1)

Positive Edge-Triggered and Negative Edge-Triggered RS Flip-Flops

The flip-flops can be positive edge triggered or negative edge triggered.

i. In positive edge-triggered flip-flops, the output responds to the R and S inputs only at the positive edges of the clock pulse. At other instants of time, the output does not change.

ii. In negative edge-triggered flip-flops, the output responds to the R and S inputs only at the negative edges of the clock pulse. At other instants of time, the output does not change.

Fig. 6 shows the input and output waveforms for positive and negative edge-triggered RS flip-flops.

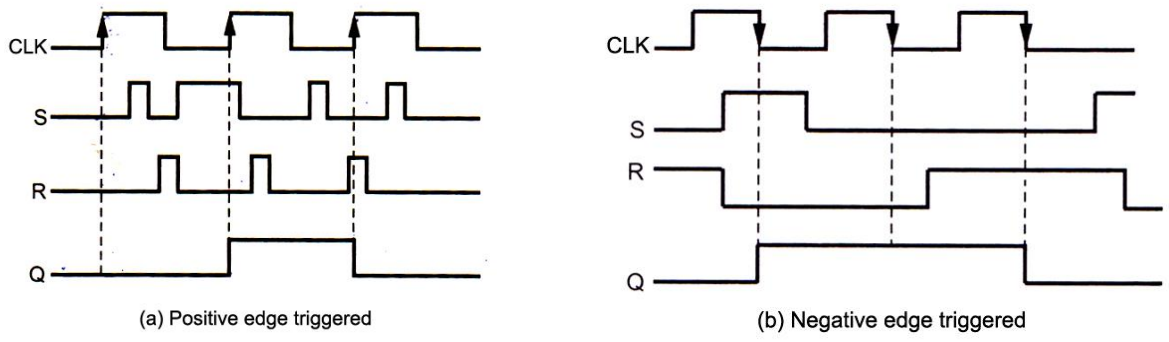


Fig. 6 Input and output waveforms for positive and negative edge-triggered RS flip-flops

IEEE Logic Symbols

Along with traditional logic symbols, the logic gates also have IEEE functional logic symbols.

Table 2 Traditional and IEEE logic gate symbols

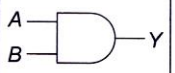
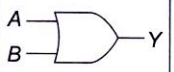
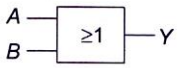
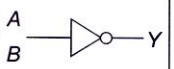
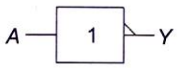
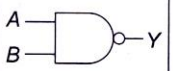
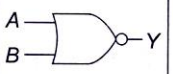
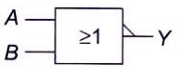
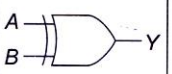
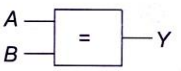
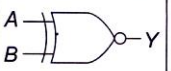
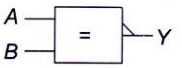
Logic Function	Traditional Logic Symbol	IEEE Logic Symbol*
AND		
OR		
NOT		
NAND		
NOR		
XOR		
XNOR		

Table 2 shows the traditional logic symbols and their IEEE counterparts. All IEEE logic symbols are rectangular and there is an identifying character or symbol inside.

Questions

1. What is a flip-flop? Distinguish between a latch and a flip-flop.
   (Dec '17 – 4M, Jun '17 – 4M, Dec '16 – 2M, Jun '16, Dec '15, Jun '15 – 4M, MQP '14 – 4M)
2. What is a latch? ***(Dec '17)***
3. With a logic diagram and truth table, explain the operation of NAND gate latch.
   (Dec '17 – 10M, Jun '17 – 8M, Jun '16 – 5M)
4. With a logic diagram and truth table, explain the operation of NOR gate latch.
   (Dec '17, Dec '16 – 5M, Jun '16 – 8M, Dec '15 – 6M, MQP '14 – 6M)
5. What is RS flip-flop? Explain its operation with circuit diagram, logic symbol and truth table.
   (Dec '17 – 6M, Jun '17 – 8M, Jun '16 – 5M, Dec '15 – 5M, Jun '15 – 6M, MQP '15 – 6M)
6. With a logic diagram and truth table, explain the operation of a clocked (or gated) RS flip-flop using NAND gates.
   (Dec '17 – 8M, Jun '17 – 8M, Dec '16 – 8M, Jun '16 – 5M, Dec '15 – 8M, Dec '14 – 6M, MQP '15 - 4M, MQP '14 – 5M)
7. Draw the traditional and IEEE logic symbols of AND, OR, NOT, NAND, NOR, XOR and XNOR. ***(MQP '15 – 4M)***

References

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